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(54) **PLANARIZERS FOR SPIN ETCH PLANARIZATION OF ELECTRONIC COMPONENTS AND METHODS OF USE THEREOF**

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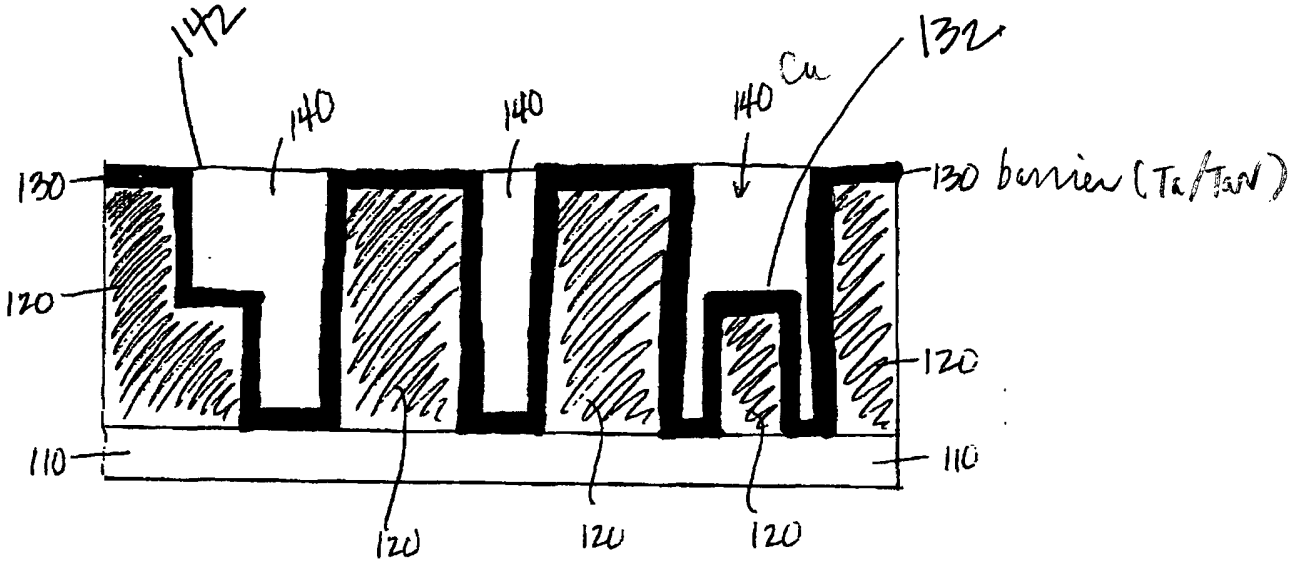
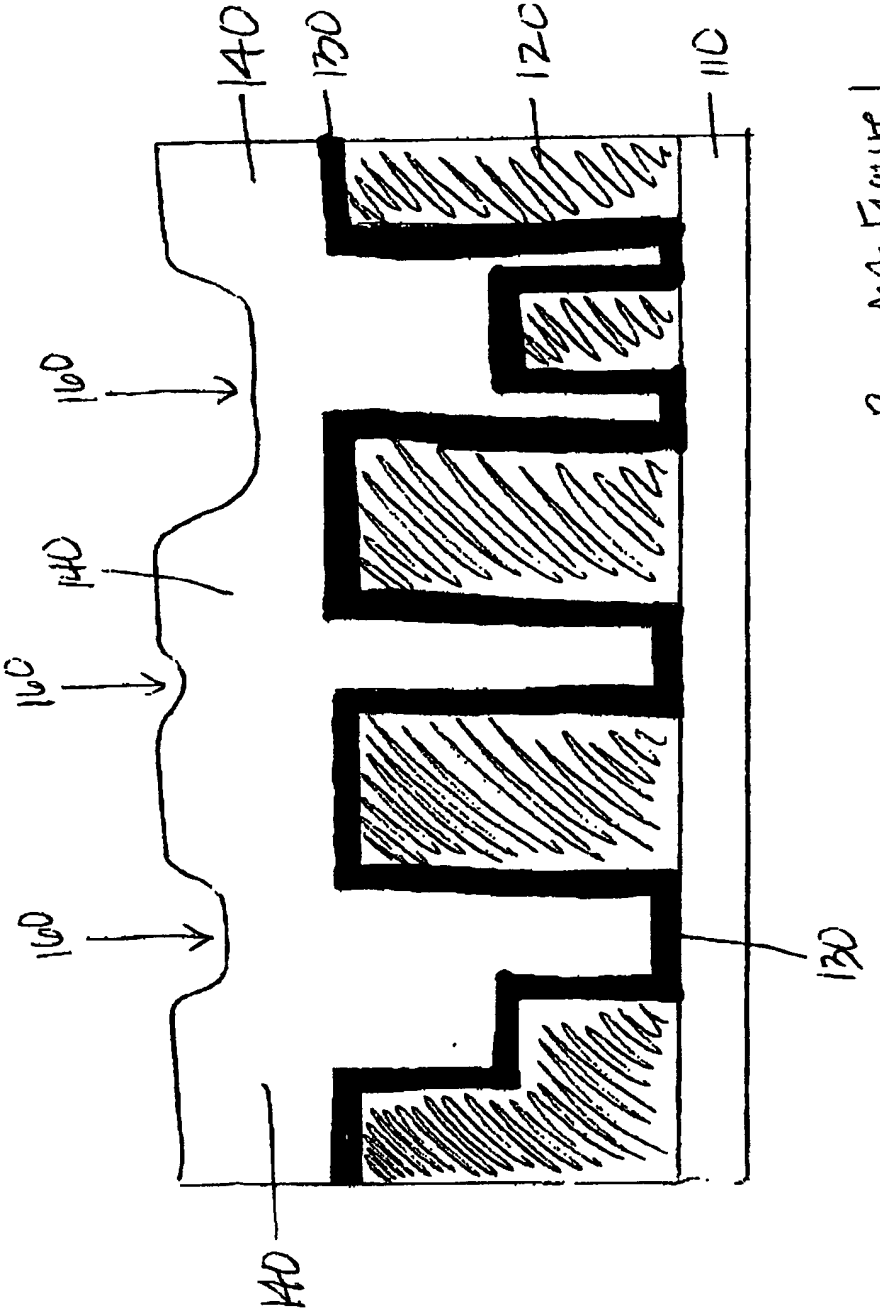
(52) **U.S. Cl.** **257/763**

(57) **ABSTRACT**

An electronic component contemplated comprises a) a substrate layer, b) a dielectric layer coupled to the substrate layer, c) a barrier layer coupled to the dielectric layer, d) a conductive layer coupled to the barrier layer, and e) a protective layer coupled to the conductive layer. The electronic component contemplated herein can be produced by a) providing a substrate; b) coupling a dielectric layer to the substrate; c) coupling a barrier layer to the dielectric layer; d) coupling a conductive layer to the barrier layer; and e) coupling a protective layer to the conductive layer. The protective layer may then be cured to a desirable hardness. A method of planarizing a conductive surface of an electronic component may comprise a) introducing or coupling a protective layer onto a conductive layer; b) dispersing the protective layer across the conductive layer; c) curing the protective layer; d) introducing an etching solution onto the conductive layer; and e) etching the conductive surface to substantial planarity.





PRIOR ART Figure 1

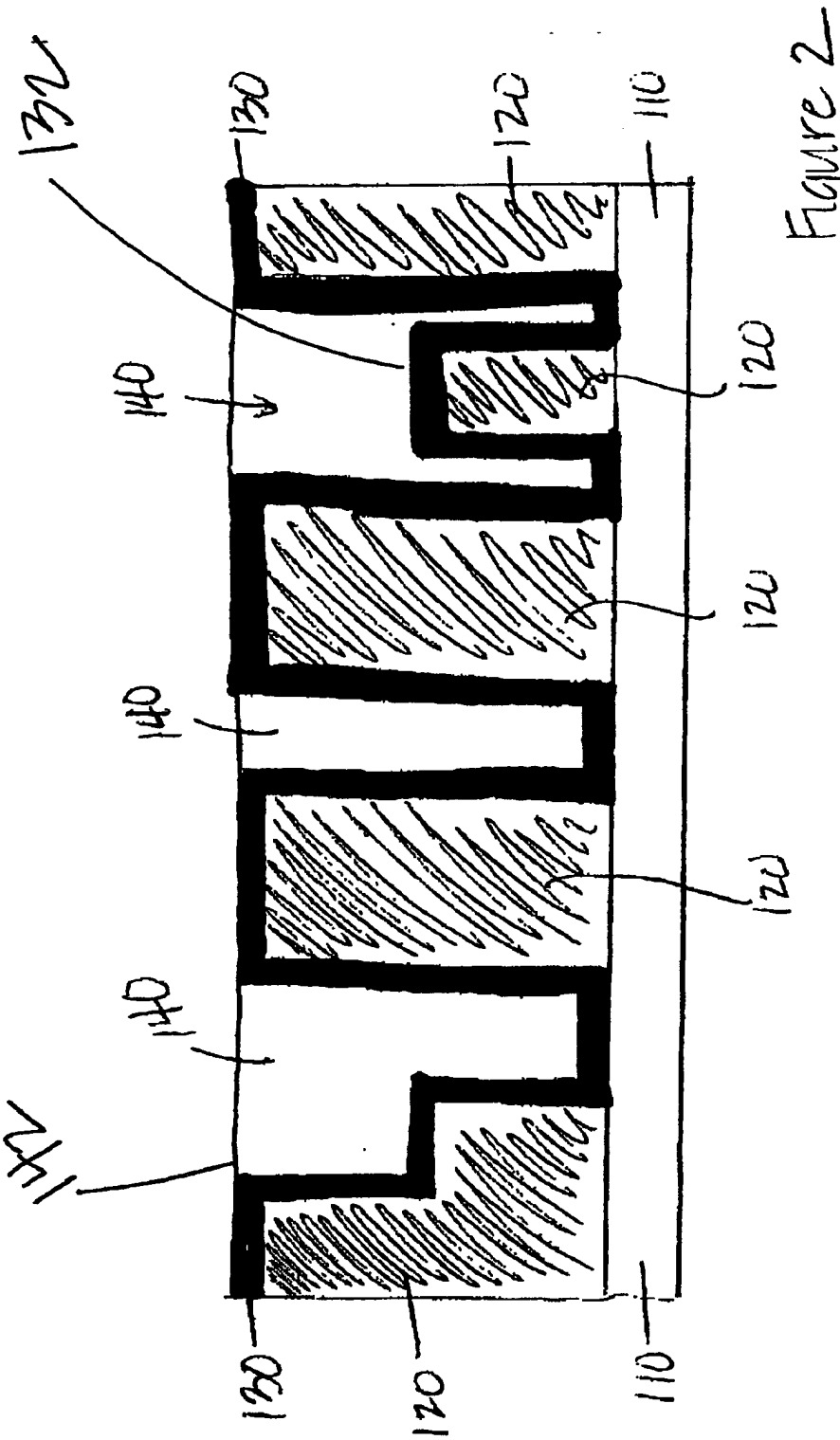


Figure 2

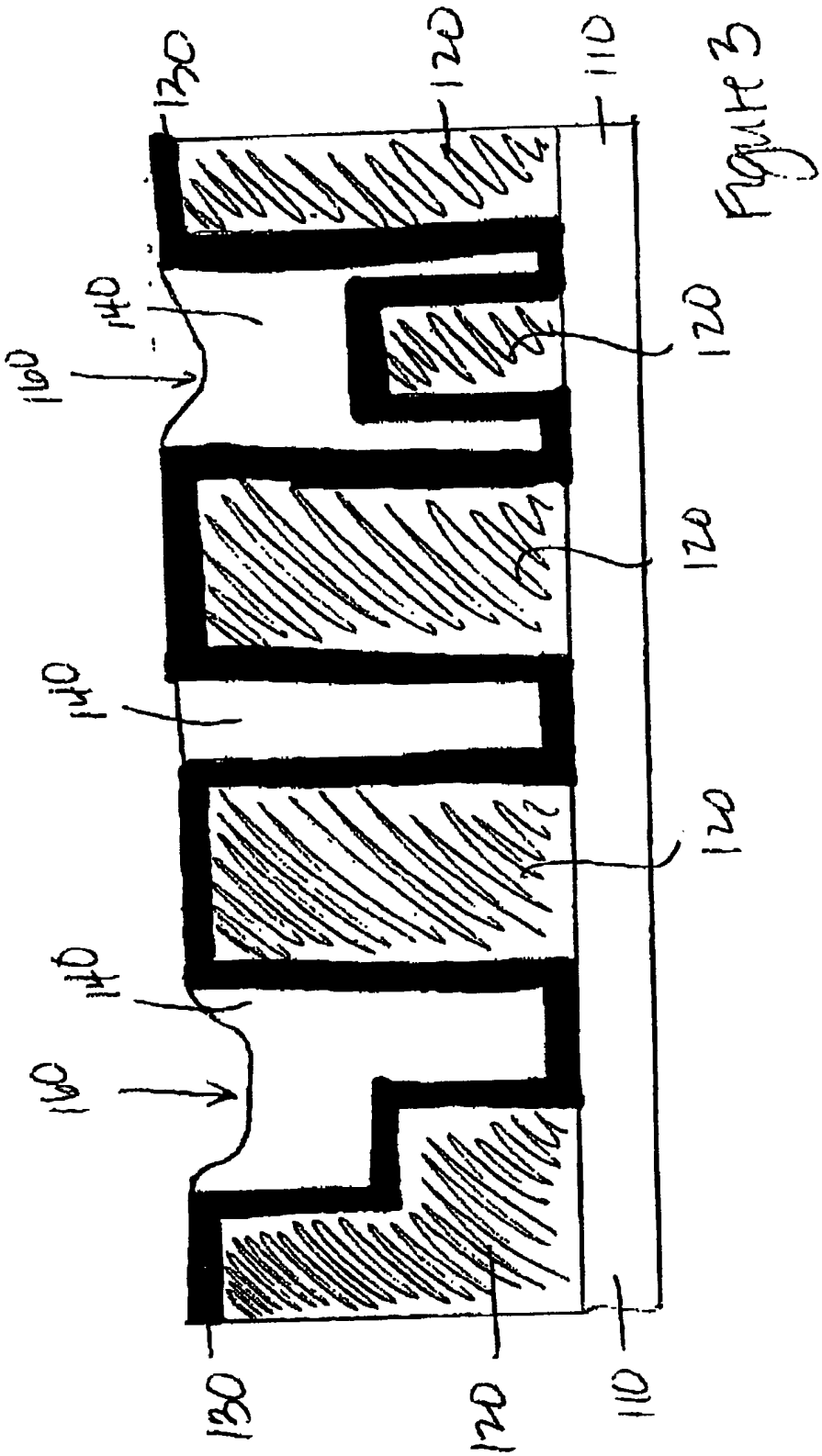


Figure 3

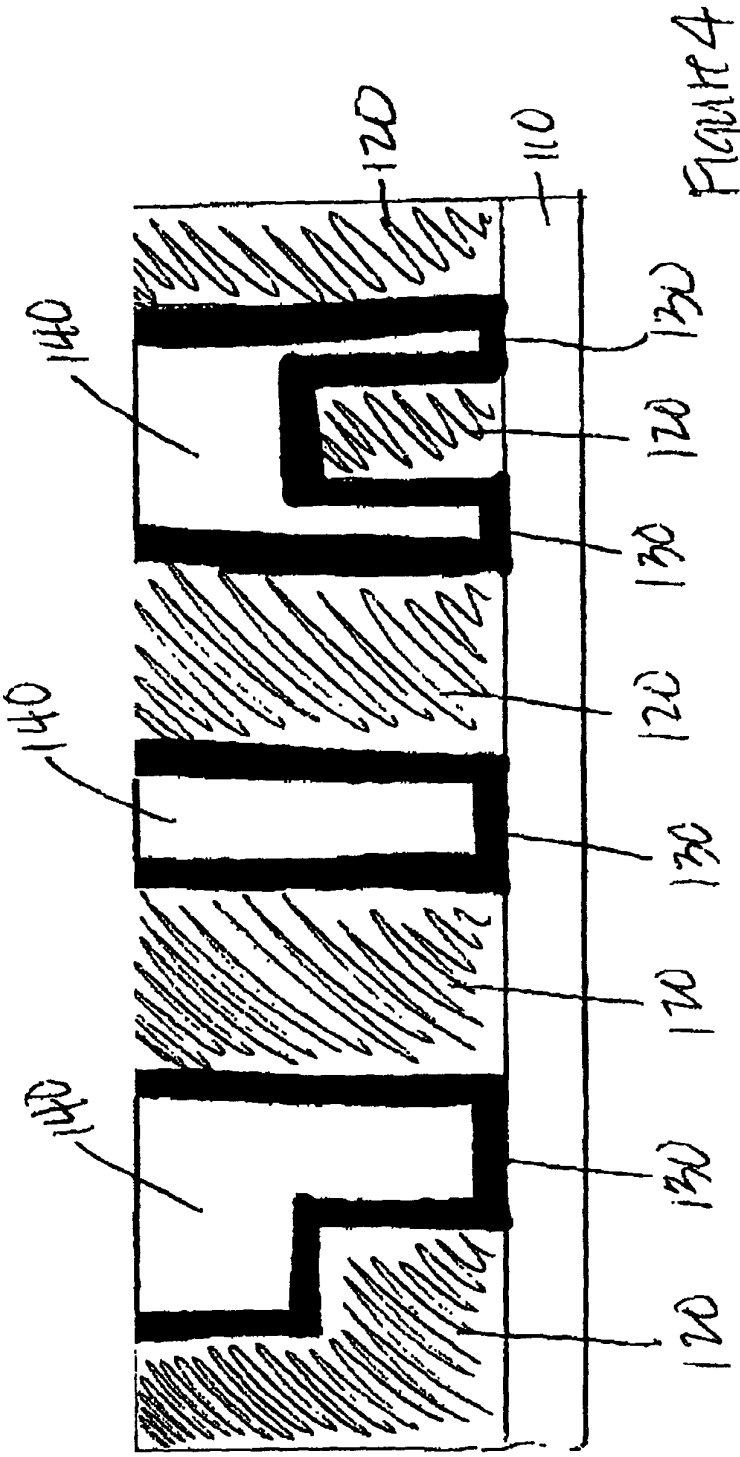


FIGURE 4

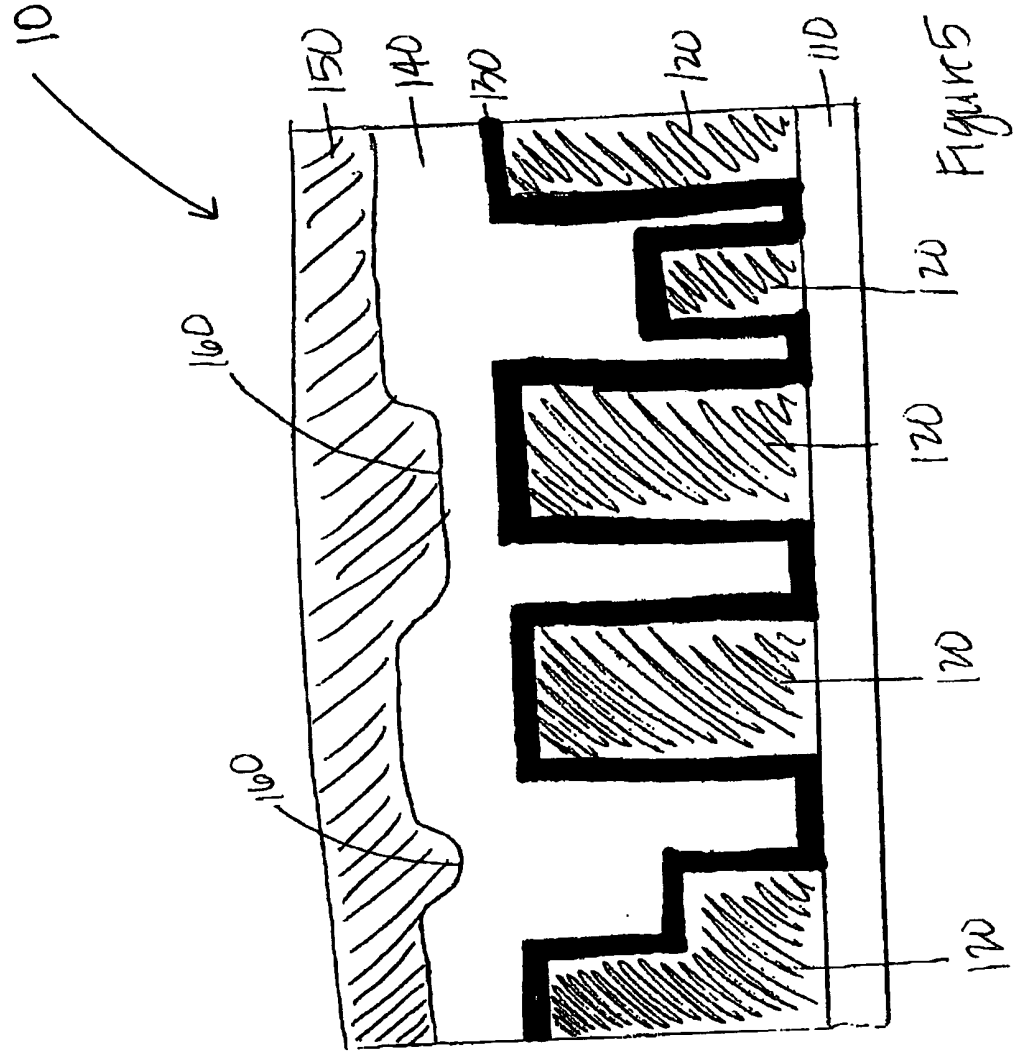


Figure 5

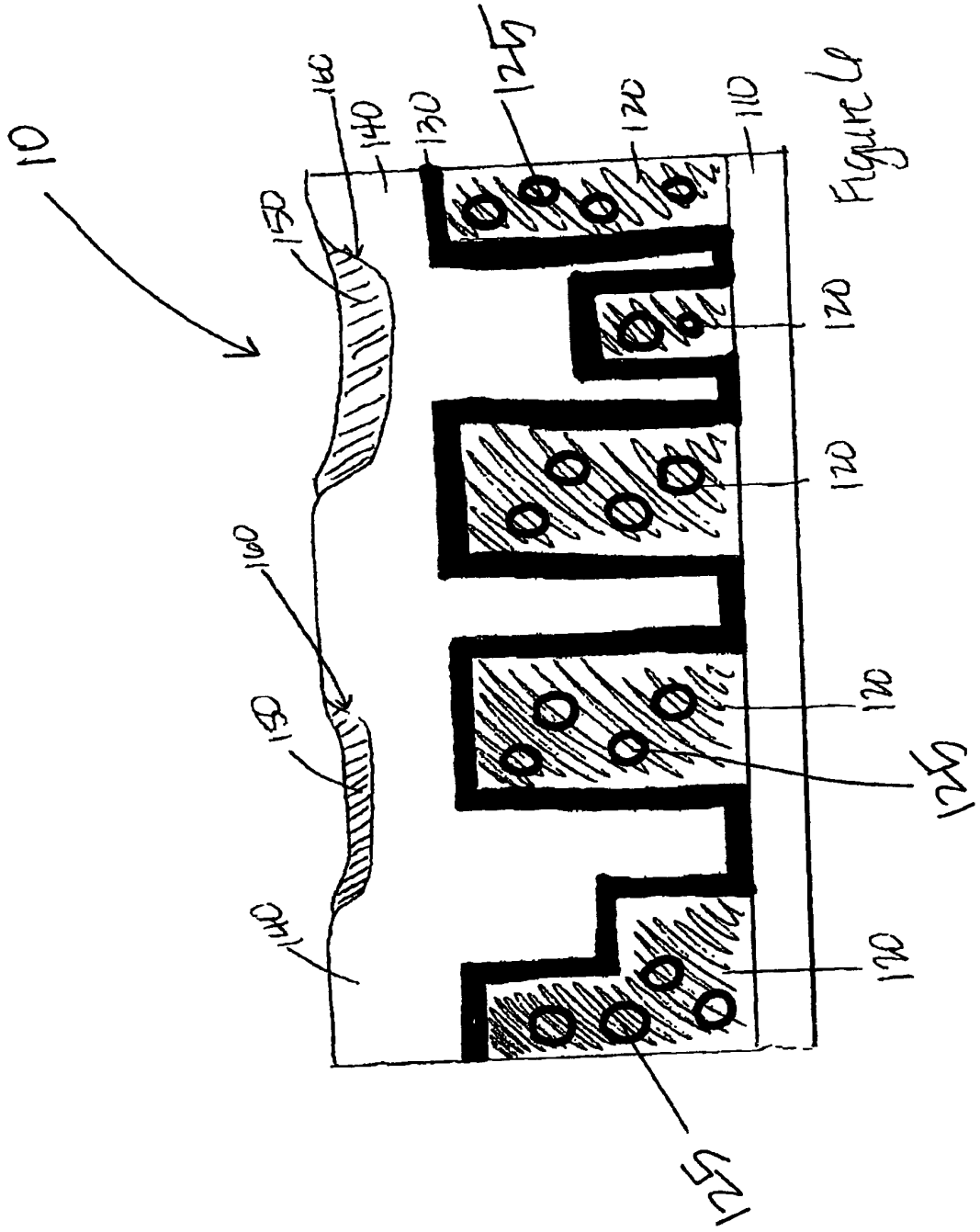


Figure 6

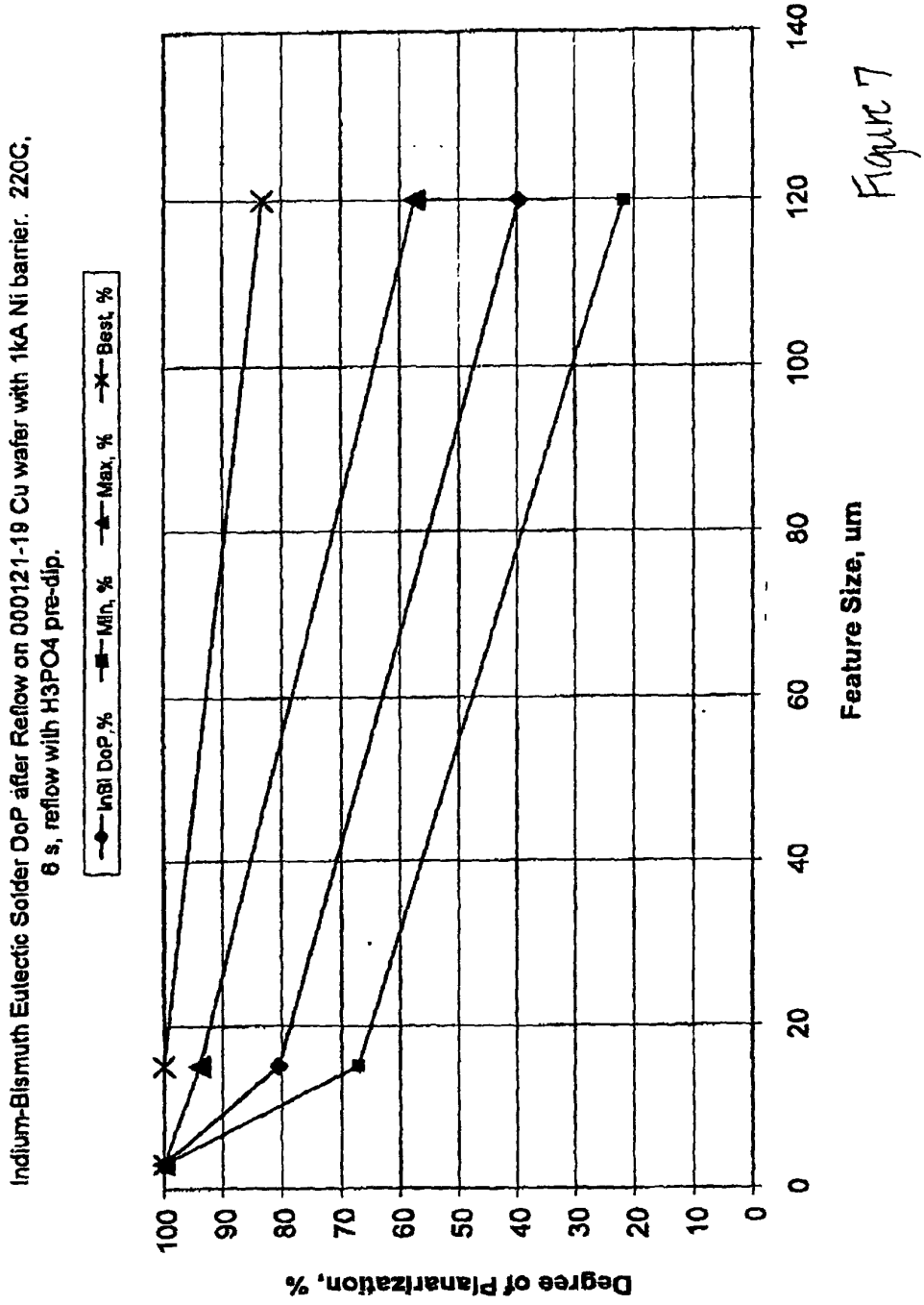

Indium-Bismuth Eutectic Solder DoP after Reflow on 000121-19 Cu wafer with 1kA Ni barrier. 220C, 8 s, reflow with H3PO4 pre-dip.
InBi DoP,%
Min, %
Max, %
Best, %
Degree of Planarization, %
100
90
80
70
60
50
40
30
20
10
0
0
20
40
60
80
100
120
140
Feature Size, um

Figure 7

PLANARIZERS FOR SPIN ETCH PLANARIZATION OF ELECTRONIC COMPONENTS AND METHODS OF USE THEREOF

[0001] This application is a continuation in part of U.S. Utility Application entitled "Viscous Protective Overlayers for Planarization" (no serial number assigned as of filing date) incorporated herein by reference in its entirety.

FIELD OF THE INVENTION

[0002] The field of the invention is planarization and electronic components.

BACKGROUND OF THE INVENTION

[0003] Electronic components are used in ever increasing numbers of consumer and commercial electronic products. Examples of some of these consumer and commercial products are televisions, computers, cell phones pagers, a palm-type organizer, portable radios, car stereos, or remote controls. As the demand for these consumer and commercial electronics increases, there is also a demand for those same products to become smaller and more portable for the consumers and businesses.

[0004] As a result of the size decrease in these products, the components that comprise the products must also become smaller. Examples of some of those components that need to be reduced in size or scaled down are printed circuit or wiring boards, resistors, wiring, keyboards, touch pads, and chip packaging.

[0005] When electronic components are reduced in size or scaled down, any defects that are present in the larger components are going to be exaggerated in the scaled down components. Thus, the defects that are present or could be present in the larger component should be identified and corrected, if possible, before the component is scaled down for the smaller electronic products.

[0006] In order to identify and correct defects in electronic components, the components, the materials used and the manufacturing processes for making those components should be broken down and analyzed. Electronic components are composed, in some cases, of layers of materials, such as metals, polymers, metal alloys, inorganic materials or organometallic materials. The layers of materials are often thin (on the order of less than a millimeter in thickness) and delicate.

[0007] As integrated circuits (ICs) become smaller and more advanced as to performance, it is imperative to increase the density of the components on the wafer, while increasing the speed at which the integrated circuit performs its functions. Increasing component density requires, among other things, decreasing the size of the conducting trenches and vias ("interconnects") on the wafer. However, decreasing the cross-section of the current-carrying conductor increases the electrical resistance for the same conducting material, which degrades circuit performance and increases heating of the interconnects. Thus, the materials and methods for producing these integrated circuits need to be evaluated and potentially replaced by better performing materials and methods of production.

[0008] Conventional IC technology uses tungsten (W) and aluminum (Al) interconnects and/or alloys containing these materials. Both tungsten and aluminum, and alloys thereof, have adequate electrical conductivity for use in electronic components, but future generations of ICs will preferably make use of higher conductivity materials, such as copper (Cu).

[0009] Copper has several advantages that make it an ideal material for use in electronic components: a) copper has the highest conductivity of any metal except pure silver, b) copper is readily solderable, c) copper has excellent corrosion resistance in natural environments. Copper alloys are also considered excellent alloys for use in electronic components. Harper, Charles A. ed., *Electronic Packaging and Interconnect Handbook*, Second Edition, McGraw-Hill (New York), 1997. Copper also has the disadvantage of being diffusive—diffusing easily and widely through other materials typically used in the fabrication of ICs, seriously degrading IC performance. To control copper diffusion into the dielectric material, especially if the dielectric material is porous, barrier materials or layers may be deposited prior to copper deposition (or deposition of any "copper-like" conductive material) to hinder diffusion of copper or another conductive material into the surrounding material or dielectric material.

[0010] Once the layered material is prepared, it is planarized to provide a flat, smooth surface that can be patterned and etched with the accuracy required of modern IC components. Contact planarization, such as Chemical Mechanical Planarization (CMP), is known in the art and fully described in textbooks, such as *Chemical Mechanical Planarization of Microelectronic Materials*, by Joseph M. Steigerwald, Shyam P. Murarka and Ronald J. Gutman (1997). CMP makes use of a polishing pad brought into mechanical contact with a wafer to be planarized with an abrasive slurry interposed between the polishing pad and the wafer. Relative motion (typically rotation) of the polishing pad with respect to the wafer leads to polishing of the wafer through mechanical abrasion. Chemical etching of the wafer then takes place through application of an etching solution to the wafer.

[0011] Non-contact planarization, such as Spin Etch Planarization (SEP), is another method of planarization whereby there is no mechanical abrasion of the surface of the wafer. The planarization process takes place purely through application of appropriate chemicals. The process of Spin Etch Planarization is described in U.S. patent application No. 09/356,487 and is incorporated by reference herein in its entirety. Aspects of non-contact planarization and Spin Etch Planarization have been reported and discussed in the following publications: J. Levert, S. Mukherjee and D. DeBear, "Spin Etch Planarization Process for Copper Damascene Interconnects" in *Proceedings of SEMI Technology Symposium* 99, Dec. 1-3, 1999, pp. 4-73 to 4-82; J. Levert, S. Mukherjee, D. DeBear, and M. Fury, "A Novel Spin-Etch Planarization Process for Dual-Damascene Copper Interconnects" in *Electrochemical Society Conference*, October 1999, p. 162 ff; and Shyama P. Mukherjee, Joseph A. Levert, and Donald S. DeBear, "Planarization of Copper Damascene Interconnects by Spin-Etch Process: A Chemical Approach" in *MRS Spring Meeting, San Francisco, Calif., Apr.* 27, 2000 and Donald S. DeBear, Joseph A. Levert, and Shyama Mukherjee, "Spin Etch Planarization for Dual Damascene

Interconnect Structures" in *Solid State Technology,* March 2000, 43(3), pp 53-60 including all of the references cited in all of the foregoing.

[0012] Non-contact planarization suffers from a considerable drawback—surface defects and imperfections are influenced by the planarization process and portions of the conductive layer in the imperfections or defect are undesirably removed resulting in a dish-like geometry. Dishing is a common and undesirable side effect of removing the field region conductive layer and the barrier layer overlying the field region. In other words, the polishing or planarization procedure wears down the tops of the imperfections but also can wear down the crevices of the imperfections, which results in a surface that contains constant imperfections despite applied planarization techniques.

[0013] Therefore, there is a need to improve planarization techniques used in the fabrication of integrated circuits, such that imperfections and surface defects in the conductive layers are not removed or are minimally removed as the surface is being planarized. Further, it is important that the improved planarization techniques do not hinder or disrupt the process of build-up of the integrated circuit.

SUMMARY OF THE INVENTION

[0014] An electronic component contemplated comprises a) a substrate layer, b) a dielectric material or layer coupled to the substrate layer, c) a barrier layer coupled to the dielectric material or layer, d) a conductive layer coupled to the barrier layer, and e) a protective layer coupled to the conductive layer.

[0015] The electronic component contemplated herein can be produced by a) providing a substrate; b) coupling a dielectric layer to the substrate; c) coupling a barrier layer to the dielectric material or layer; d) coupling a conductive layer to the barrier layer; and e) coupling a protective layer, which planarizers or can be planarized, to the conductive layer. The protective layer may then be cured to a desirable hardness.

[0016] A method of planarizing a conductive surface of an electronic component may comprise a) introducing or coupling a protective layer onto a conductive layer; b) dispersing and planarizing the protective layer across the conductive layer; c) curing the protective layer; d) introducing an etching solution onto the conductive layer; and e) etching the conductive surface to substantial planarity.

[0017] Various objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of preferred embodiments of the invention, along with the accompanying drawings in which like numerals represent like components.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] **FIG. 1** is a schematic diagram of a conventional damascene metal interconnection structure before planarization.

[0019] **FIG. 2** is a schematic diagram of a conventional component where the surface is polished and all imperfections are removed.

[0020] **FIG. 3** is a schematic diagram showing a conventional layered material.

[0021] **FIG. 4** is a schematic diagram of a conventional layered material where the barrier layer is removed after its exposure by subsequent planarization along with removal of sufficient conductive material or layer to retain coplanarity of the metal-filled feature and dielectric.

[0022] **FIG. 5** is a schematic diagram of a contemplated embodiment of the present invention.

[0023] **FIG. 6** is a schematic diagram of a contemplated embodiment of the present invention.

[0024] **FIG. 7** is a graph showing the Degree of Planarization versus the Feature Size in micrometers.

DETAILED DESCRIPTION

[0025] Prior art **FIG. 1** shows a schematic diagram of a conventional damascene metal interconnection structure before planarization comprising a) a substrate layer **110**, b) a dielectric material or layer **120** coupled to the substrate layer **110**, c) a barrier layer **130** coupled to the dielectric layer **120** and d) a conductive layer **140** coupled to the barrier layer **130**. This type of conventional interconnection structure might be found in several types of typical electronic components.

[0026] The dielectric material or layer **120** in **FIG. 1** is usually patterned by techniques such as photolithography, and plasma etching. (Note: the terms "dielectric material" and "dielectric layer" are intended to be used interchangeably throughout this disclosure). The barrier layer **130** is typically deposited on the patterned dielectric followed by deposition of the conductive layer **140**. Conventional barrier layers **130** comprise tantalum/tantalum nitride (Ta/TaN) and are used with copper conductive layers **140**.

[0027] The conductive layer in these conventional components contains imperfections that can be significant problems when building a layered component. **FIG. 1** shows what imperfections **160** might look like on the surface of the conductive layer **140**. Surface topography imperfections are created because of the conformal application of the conductive layer to the surface topography of trenches and vias formed by the underlying barrier material and dielectric material.

[0028] Ideally, to correct the imperfections **160** in a conventional electronic component, the surface of the conductive layer is planarized or polished by some means, such as mechanical polishing, chemical polishing, or chemical mechanical polishing. **FIG. 2** shows an ideal situation where the surface is polished and all imperfections are removed. Perfect planarization removes copper until the upper or elevated surface **142** of the conductive layer **140** is co-planar with the upper surface **132** of the barrier layer **130** on the field region, and at that point, etching is halted. Ideal planarization also removes the barrier layer **130** at the same rate as the conductive layer **140**—substantially a 1 to 1 selectivity.

[0029] Realistically, however, as the surface is being planarized, the imperfections **160** in the conductive layer **140** are influenced by the planarization process and portions of the conductive layer **140** in the imperfections **160** are undesirably removed resulting in a dish-like geometry, which is termed "dishing". The imperfections **160** can be created through dishing and by surface topography defects.

Dishing is a result of a non-efficient planarization process during removal of excess conductive material. (See **FIG. 3**). Dishing is a common and undesirable side-effect of removing the field region conductive layer **140** and the barrier layer **130** overlying the field region. In other words, the polishing or planarization procedure wears down the tops of the imperfections but also can wear down the crevices of the imperfections. Further, the etchants being used frequently do not remove the barrier layer **130** at the same rate as the conductive layer **140**, which contributes to additional formation of surface defects.

[0030] **FIG. 4** shows another conventional layered material where the barrier layer **130** is removed after its exposure by subsequent planarization along with removal of sufficient conductive material or layer **140** to retain coplanarity of the metal-filled feature and dielectric layer **120**. If the planarization procedure achieves substantially a 1:1 selectivity in the removal of barrier material **130** and conductive layer **140**, the direct planarization may be accomplished in one step. However, this is quite an idealistic achievement for any planarization process. Any practical planarization process, such as the one disclosed herein, must take into consideration the effects of dishing and surface topography defects.

[0031] **FIG. 5** shows a preferred embodiment of an electronic component **10** contemplated herein comprising a) a substrate layer **110**, b) a dielectric layer **120** coupled to the substrate layer **110**, c) a barrier layer **130** coupled to the dielectric layer **120**, d) a conductive layer **140** coupled to the barrier layer **130**, and e) a protective layer **150** coupled to the conductive layer **140**.

[0032] As used herein, the term "electronic component" means that component that is part of an electronic device, such as a circuit board, a capacitor, a resistor, chip packaging, a layered integrated circuit or an inductor. It is preferred that the electronic component **10** comprises a circuit board or layered integrated circuit.

[0033] The substrate layer **110**, in this embodiment, is designed to a) be functional within the electronic component **10** and b) provide support to the dielectric layer **120**. The substrate can comprise virtually any substance upon which a compound or dielectric material can be deposited, as well as repeating layers like the layered structures contemplated herein. For example, contemplated substrates include metals and non-metals, conductors and non-conductors, flexible and inflexible materials, absorbent and non-absorbent materials, flat and curved materials, textured and non-textured materials, and both large and small objects. Particularly preferred substrates are circuit boards, paper, glass, and metal objects. In preferred embodiments, the substrate comprises silicon, silicon-germanium, gallium-arsenide, indium phosphide, quartz, or sapphire wafer, with the silicon wafer being the most preferred.

[0034] The phrase "dielectric constant" means a dielectric constant evaluated at 1 MHz to 2 GHz for a material, unless otherwise inconsistent with context. It is contemplated that the value of the dielectric constant of the dielectric layer **120** is less than 3.0. In a preferred embodiment, the value of the dielectric constant is less than 2.5, and in still more preferred embodiments, the value of the dielectric constant is less than 2.0.

[0035] The dielectric material or dielectric layer **120** (both the terms "dielectric material" and "dielectric layer" can be used interchangeably) can be designed to satisfy several design goals, such as providing support for the substrate layer **110** and the barrier layer **130**, while maintaining a relatively low dielectric constant. The dielectric layer **120** can be coupled to the substrate layer **110** by any suitable process, such as use of an adhesive, hydrogen bonding, electrostatic interactions, Van der Waals forces, and coulombic interactions. The dielectric material **120** may also either be porous or non-porous depending on the structural, electrical, and dielectric needs of the component.

[0036] Porous dielectric layers **120**, as shown incorporated into an electronic component **10** in **FIG. 6**, are dielectric layers that contain both a solid component, such as an organic, inorganic or organometallic compound, and a plurality of voids. As used herein, the word "void" means a volume in which a mass is replaced with a gas. The composition of the gas is generally not critical, and appropriate gases include relatively pure gases and mixtures thereof, including air. Voids **125** are typically spherical, but may alternatively or additionally have any suitable shape, including tubular, lamellar, discoidal, or other shapes. It is also contemplated that voids **125** may have any appropriate diameter. It is further contemplated that at least some voids **125** may connect with adjacent voids **125** to create a structure with a significant amount of connected or "open" porosity. Voids **125** preferably have a mean diameter of less than 1 micrometer, and more preferably have a mean diameter of less than 100 nanometers, and still more preferably have a mean diameter of less than 10 nanometers. It is further contemplated that voids **125** may be uniformly or randomly dispersed within the dielectric layer **120**. In a preferred embodiment, voids **125** are uniformly dispersed within the dielectric layer **120**.

[0037] The dielectric material or layer **120** can be composed of inorganic, organic, or organometallic compounds, as well as mixtures of these materials. Examples of contemplated inorganic compounds are silicates, aluminates and compounds containing transition metals. Examples of organic compounds include polyarylene ether, polyimides and polyesters. Examples of contemplated organometallic compounds include poly(dimethylsiloxane), poly(vinylsiloxane) and poly(trifluoropropylsiloxane).

[0038] The dielectric material **120** may also include substantially polymeric material, substantially monomeric material or a mixture of both polymers and monomers depending on the desired final dielectric composition, desired electrical properties, and desired use of the dielectric material. It is further contemplated that the dielectric material **120** may be composed of amorphous, cross-linked, crystalline, or branched polymers. Preferred components of the dielectric material **120** are inorganic polymers. More preferred components of the dielectric material **120** are inorganic, cross-linked polymers because of the increased durability and polymer strength. The term "crosslinking" refers to a process in which at least two molecules, or two portions of a long molecule, are joined together by a chemical interaction. Such interactions may occur in many different ways, including formation of a covalent bond, formation of hydrogen bonds, hydrophobic, hydrophilic, ionic or electrostatic interaction. Furthermore, molecular interaction may also be characterized by an at least temporary physical connection between a molecule and itself or between two or more molecules.

[0039] Contemplated polymers may also comprise a wide range of functional or structural moieties, including aromatic systems, and halogenated groups. Furthermore, appropriate polymers may have many configurations, including a homopolymer, and a heteropolymer. Moreover, alternative polymers may have various forms, such as linear, branched, super-branched, or three-dimensional. The molecular weight of contemplated polymers spans a wide range, typically between 400 Dalton and 400000 Dalton or more. In a preferred embodiment, the dielectric material **120** comprises inorganic molecules or polymers. In a most preferred embodiment, the dielectric material **120** comprises a polysilicate.

[0040] The dielectric material **120** may additionally or alternately comprise monomers in order to meet certain design goals and/or structural requirements. As used herein, the term "monomer" refers to any chemical compound that is capable of forming a covalent bond with itself or a chemically different compound in a repetitive manner. The repetitive bond formation between monomers may lead to a linear, branched, super-branched, or three-dimensional product. Furthermore, monomers may themselves comprise repetitive building blocks, and when polymerized the polymers formed from such monomers are then termed "block-polymers". Monomers may belong to various chemical classes of molecules including organometallic or inorganic molecules. Examples of contemplated organometallic monomers are octamethylcyclotetrasiloxane, methylphenylcyclotetrasiloxane, hexanethyldisilazane, and triethyoxysilane. Examples of contemplated inorganic monomers include tetraethoxysilane or aluminum isopropoxide. The molecular weight of monomers may vary greatly between about 40 Dalton and 20000 Dalton. However, especially when monomers comprise repetitive building blocks, monomers may have even higher molecular weights. Monomers may also include additional groups, such as groups used for crosslinking.

[0041] In further alternative embodiments, many other silicon-containing materials are contemplated as components of the dielectric material **120**, including colloidal silica, fumed silica, siloxanes, silsequioxanes, and sol-gel-derived monosize silica. Appropriate silicon-containing compounds preferably have a size of below 100 nm, more preferably below 10 nm and most preferably below 5 nm. It is also contemplated that the dielectric material **120** may comprise materials other than silicon- containing materials, including organic, organometallic or partially-inorganic materials, provided that such materials can be dissolved at least in part in a solvent that does not dissolve the dielectric material **120**. For example, appropriate organic materials are polystyrene, and polyvinyl chloride. Contemplated organometallic materials are, for example, octamethylcyclotetrasiloxane. Contemplated inorganic materials are, for example, KNO_3.

[0042] Alternatively, the organic and inorganic compounds can be selected such that the inorganic component can be dissolved at least in part by a solution that does not dissolve the organic component of the dielectric material **120**. For example, colloidal silica can be dissolved by a dilute HF solution without dissolving an organic polymer such as polyarylene ether.

[0043] In some preferred embodiments, dielectric material **120** may comprise dielectric materials contemplated, produced or disclosed by Honeywell, Inc. including, but not limited to: a) FLARE (poly(arylene ether)), such as those compounds disclosed in issued patents U.S. Pat. No. 5,959,157, U.S. Pat. No. 5,986,045, U.S. Pat. No. 6,124,421, U.S. Pat. No. 6,156,812, U.S. Pat. No. 6,172,128, U.S. Pat. No. 6,171,687, U.S. Pat. No. 6,214,746, and pending application Ser. Nos. 09/197478, 09/538276, 09/544504, 09/741634, 09/651396, 09/545058, 09/587851, 09/618945, 09/619237, 09/792606, b) GX3 (adamantane-based materials), such as those shown in pending application Ser. No. 09/545058, c) nanoporous silica materials and silica-based compounds, such as those compounds disclosed in issued patents U.S. Pat. No. 6,022,812, U.S. Pat. No. 6,037,275, U.S. Pat. No. 6,042,994, U.S. Pat. No. 6,048,804, U.S. Pat. No. 6,090,448, U.S. Pat. No. 6,126,733, U.S. Pat. No. 6,140,254, U.S. Pat. No. 6,204,202, U.S. Pat. No. 6,208,014, and pending application Ser. Nos. 09/046474, 09/046473, 09/111084, 09/360131, 09/378705, 09/234609, 09/379866, 09/141287, 09/379484, 09/392413, 09/549659, 09/488075, 09/566287, and 09/214219 all of which are incorporated by reference herein in their entirety.

[0044] A barrier layer **130** is coupled to the dielectric material **120** by any suitable process, such as use of an adhesive, hydrogen bonding, electrostatic interactions, Van der Waals forces, and coulombic interactions. The barrier layer **130** may comprise any suitable material or materials that is capable of meeting several and sometimes conflicting design goals, such as a) successfully protecting the dielectric layer **120** from any diffusion of the conductive layer **140**, b) acting as an "etch stop"—which indicates the end point of the conductive field planarization step, c) reacting to etching chemicals in a 1 to 1 selectivity rate with the conductive layer materials **140**, and/or d) not reacting to the etching chemicals at all, such that when the etching chemicals reach the barrier layer **130** none of the barrier layer **130** is removed. Contemplated barrier layers **130** comprise tantalum, tantalum nitride, titanium, titanium nitride, tungsten-nitride, tungsten cobalt phosphorus, and nickel. In preferred embodiments, the barrier layer **130** comprises tantalum, tantalum nitride, or tantalum/tantalum nitride (Ta/TaN) stacks.

[0045] A conductive layer **140** is applied to and coupled to the barrier layer **130** by any suitable deposition method, such as electrodeposition, chemical vapor deposition (CVD), plasma vapor deposition (PVD), and fill deposition. Fill deposition, as used herein, is a process where the conductive layer **140** is applied to fill the interconnect features (vias and trenches) and to coat the flat "field" regions between features leading to a conductive layer **140** covering the entire dielectric layer **120** and the barrier layer **130**. Fill deposition typically results in a non-planar surface topography of the conductive layer **140** because of the variation of the size of the underlying dielectric layer **120** features being coated or filled.

[0046] Conductive layers **140** may generally comprise metals, metal alloys, conductive polymers, conductive composite materials, and any other suitable conductive materials. As used herein, the term "metal" means those elements that are in the d-block and f-block of the Periodic Chart of the Elements, along with those elements that have metal-like properties, such as silicon and germanium. As used herein, the phrase "d-block" means those elements that have electrons filling the *3d*, *4d*, *5d*, and *6d* orbitals surrounding the

nucleus of the element. As used herein, the phrase "f-block" means those elements that have electrons filling the *4f* and *5f* orbitals surrounding the nucleus of the element, including the lanthanides and the actinides. Preferred metals include titanium, silicon, cobalt, copper, nickel, iron, zinc, vanadium, aluminum, tin, chromium, platinum, palladium, gold, silver, tungsten, molybdenum, cerium, promethium, and thorium. More preferred metals include aluminum, titanium, silicon, copper, nickel, platinum, tin, gold, silver and tungsten. Most preferred metals include copper, aluminum and tungsten. The term "metal" also includes alloys, metal/metal composites, metal ceramic composites, metal polymer composites, as well as other metal composites.

[0047] The protective layer **150** is coupled to the conductive layer **140** by any suitable process, such as use of an adhesive, hydrogen bonding, electrostatic interactions, Van der Waals forces, and coulombic interactions.

[0048] The protective layer **150** is also generally contemplated to be a protective or passivating overlayer, which planarizes or can be planarized and that is coupled to the conductive layer **140** initially or at some stage of processing as a liquid, but may be converted into a harder or solid protective layer upon application of a curing process. The protective layer **150** can be deposited onto the conductive layer **140** by a variety of processes, including electroplating, spin-on deposition, evaporative deposition, electroless plating, sputtering/PVD, PECVD, CVD, and/or vacuum evaporation with or without a voltage bias.

[0049] The protective layer **150** can be composed of inorganic, organic, or organometallic compounds, metals and metal alloys as well as mixtures of these materials. Contemplated inorganic and organic compounds should be those compounds that are a) capable of being controllably etchable at the same time that the coupled conductive layer **140** is being etched, and b) planarizes on the conductive layer **140** before the etching step begins. Planarizing on the conductive layer **140** may comprise either a) a material that melts with a low viscosity and a high surface tension that can flow to form on the conductive layer **140** and/or b) can self-catalyze or self-cure to the desirable hardness on the conductive layer **140** after being applied to the conductive layer **140**, or a fluid material that can be mechanically planarized. (See "Improved Apparatus and Methods for Integrated Circuit Planarization", Endisch, Levert et al.; contact planarization device and apparatus). Examples of contemplated inorganic compounds are silicates, aluminates, siloxane compounds, HOSP compounds, such as those that are commercially available from Honeywell International, Inc. or disclosed in commonly assigned U.S. Pat. Nos. 6,020,410, 6,043,330, 5,973,095 incorporated by reference herein in their entirety, Spin-on Glass compounds, such as Honeywell 512B, and compounds containing transition metals. Examples of organic compounds include polyarylene ether (FLARE materials), polyimides, Accuflow mixtures (Novalac Resins), acrylic polymers, polyvinyl acetates, PMMA, polyoctadecyl methacrylate, polyvinyl pyridine, Superglues (cyanoacrylates), PVB (polyvinyl buterol) and polyesters. Examples of contemplated organometallic compounds include poly(dimethylsiloxane), poly(vinylsiloxane) and poly(trifluoropropylsiloxane). Examples of contemplated metals and metal alloys include copper; liquid metals, such a mercury; lead free solder, tin, tin etchant ($HCl+HNO_3$), gallium and gallium alloys, and bismuth and bismuth alloys (including those with indium), indium and indium alloys.

[0050] The protective layer **150** may also include substantially polymeric material, substantially monomeric material or a mixture of both polymers and monomers depending on the desired viscous consistency, the desired final consistency if curing is applied to the protective layer, and the desired planarization and etch properties. It is further contemplated that the protective layer **150** may be composed of amorphous, cross-linked, crystalline, or branched polymers.

[0051] Contemplated polymers may also comprise a wide range of functional or structural moieties, including aromatic systems, and halogenated groups. Furthermore, appropriate polymers may have many configurations, including a homopolymer, and a heteropolymer. Moreover, alternative polymers may have various forms, such as linear, branched, super-branched, or three-dimensional. The molecular weight of contemplated polymers spans a wide range, typically between 400 Dalton and 400000 Dalton or more. In a preferred embodiment, the protective layer **150** comprises inorganic molecules or polymers. In a most preferred embodiment, the protective layer **150** comprises a polysilicate.

[0052] The protective layer **150** may additionally or alternately comprise monomers in order to meet certain design goals and/or structural requirements, such as those mentioned previously. Monomers may belong to various chemical classes of molecules including organometallic or inorganic molecules. Examples of contemplated organometallic monomers are octamethylcyclotetrasiloxane, methylphenylcyclotetrasiloxane, hexanethyldisilazane, and triethyoxysilane. Examples of contemplated inorganic monomers include tetraethoxysilane or aluminum isopropoxide. Monomers may also include additional groups, such as groups used for crosslinking.

[0053] In further alternative embodiments, many other silicon-containing materials are contemplated as components of the protective layer **150**, including colloidal silica, fumed silica, siloxanes, silsequioxanes, and sol-gel-derived monosize silica. Appropriate silicon-containing compounds preferably have a size of below 100 nm, more preferably below 10 mn and most preferably below 5 nm. Preferred silicon-containing compounds include Honeywell spin-on glass materials, such as Honeywell 314 and Honeywell 512B.

[0054] The protective layer **150** may also comprise low temperature melting metals or metal alloys, preferably lead free, and will generate environmentally benign etching byproducts. A protective layer **150** comprising these metals or metal alloys must have a melting temperature below 400° C., which is considered the thermal budget of the wafer. Contemplated metals or metal alloys must not rapidly form alloys or intermetallic compounds with the existing conductive layer **140** onto which they have been deposited. An additional barrier layer can be deposited over the conductive copper layer, as part of the protective layer, to prevent liquid of solid-state diffusion of the overlayer metal into the conductive material. Nickel is an example of a material that has successfully prevented this type of diffusion into the conductive layer, which could damage the final electrical properties of the conductive layer.

[0055] An electronic component **10** can be produced by a) providing a substrate **110**; b) coupling a dielectric layer **120** to the substrate **110**; c) coupling a barrier layer **130** to the dielectric layer **120**; d) coupling a conductive layer **140** to the barrier layer **130**; and e) coupling a protective layer **150** to the conductive layer **140**. The protective layer **150** may then be cured to a desirable hardness.

[0056] The barrier layer **130** can be deposited onto the dielectric layer, the conductive layer **140** can be deposited on the barrier layer **130** and the protective layer **150** can be deposited onto the conductive layer **140** by a variety of processes, including electroplating, spin-on deposition, evaporative deposition, electroless plating, sputtering/PVD, PECVD, CVD, and/or vacuum evaporation with or without a voltage bias.

[0057] The protective layer **150** can be cured either by a process external to the material in the protective layer **150** or may be cured by a process internal to the material in the protective layer **150**. External processes include but are not limited to heat, radiation, air flow, pressure, and decrease in temperature. Internal processes are those processes that take place within the compound itself, such as crosslinking, chemical reactions between constituents that are not initiated by outside forces and other related processes.

[0058] A method of planarizing a conductive layer **150** of an electronic component **10** may comprise a) introducing or coupling a protective layer **140** onto a conductive layer **150**; b) dispersing and planarizing the protective layer **150** across the conductive layer **140**; c) curing the protective layer **150**; d) introducing an etching solution **170** (not shown) onto the conductive layer **140**; and e) etching the conductive layer **140** to substantial planarity.

[0059] Introducing or coupling the protective layer **150** onto the conductive layer **140** can be achieved by a variety of processes, including electroplating, spin-on deposition, evaporative deposition, electroless plating, sputtering/PVD, PECVD, CVD, and/or vacuum evaporation with or without a voltage bias. It is contemplated that the protective layer **150** will be introduced onto the conductive surface **140** in such quantities that preferential protection to depressed regions of the conductive surface **140** will be accomplished.

[0060] Dispersing the protective layer **150** across the conductive layer **140** is accomplished through relative motion of the electronic component **10**. Relative motion is contemplated to mean spinning the component **10**, shaking the component **10**, rocking the component **10**, or otherwise moving the component **10** around to disperse the protective layer **150**.

[0061] Curing the protective layer **150** is contemplated to encompass the methods previously discussed herein, including external and internal curing processes. External processes include but are not limited to heat, radiation or irradiation, air flow, pressure, ashing (exposure to an oxygen or oxygen-mixture with nitrogen, hydrogen or forming gas plasma), a decrease in temperature or a combination of any of the above-mentioned curing processes. Internal processes are those processes that take place within the compound itself, such as crosslinking, chemical reactions between constituents that are not initiated by outside forces and other related processes.

[0062] Introducing the etching solution **170** (not shown) onto the conductive layer **140** may be accomplished by any suitable means, including spin-on deposition, random deposition, surface washing, dipping, dripping, and rolling the etching solution **170** onto the surface. Typical and contemplated etching solutions comprise one or more of the following: HNO_3, H_3PO_4, CH_3COOH, HCl, chlorides of copper and zinc, HBr, H_2SO_4 and HF. Preferred etching solutions comprise: a) 69 weight % (wt %)//10 volume % (vol %) HNO_3, 85 wt %/50 vol % H_3PO_4, and 98 wt %/40 vol % CH_3COOH; b) 69 weight % (wt %)/6 volume % (vol %) HNO_3, 85 wt %/70 vol % H_3PO_4, and 98 wt %/24 vol % CH_3COOH; 69 weight % (wt %)/1.6 volume % (vol %) HNO_3, 85 wt %/53.9 vol % H_3PO_4, and 98 wt %/43.2 vol % CH_3COOH; 49 wt %/1.3 vol % HF.

[0063] As used herein, the phrase "substantial planarity" generally means that degree of planarity that is considered to be acceptable for the contemplated or desired electronic component. Substantial planarity is considered herein to be a degree of planarity of at least 0.6 or 60% or achieving perfect planarity. In preferred embodiments, substantial planarity is considered to be a degree of planarity of at least 0.8 or 80%. And in more preferred embodiments, substantial planarity is considered to be a degree of planarity of at least 0.9 or 90%. Analytical Test Methods: Planarization was measured by KLA-Tencor HRP-220 mechanical stylus profilometer.

EXAMPLES

Example 1

[0064] Planarizer Material/Protective Layer Deposition

[0065] A 1000 Angstrom thick nickel barrier layer is deposited on a copper substrate/conductive layer by vacuum evaporation. A planarizer material/protective layer comprising 66.3 wt % Indium and 33.7 wt % of Bismuth as a eutectic alloy is deposited on the barrier layer by vacuum evaporation to a thickness of 1.5 μm. Both the nickel barrier layer and indium bismuth protective layer are deposited by using a vacuum evaporative deposition tool to form a wafer. This deposition tool uses electron beam evaporation of any elemental or alloy metal allowing deposition under a vacuum atmosphere. The copper substrate/conductive layer surface was precleaned with an argon sputter using a voltage bias before the nickel barrier layer and the indium bismuth protective layer were deposited. Both the nickel barrier layer and the indium bismuth protective layer were deposited without "breaking" or turning off the vacuum after precleaning.

[0066] The barrier layer and the conductive layer discussed above may also be deposited also by electroplating and electroless plating, which are both economical methods. Electroplating is a simple scale-up from existing copper plating technology used today by the integrated circuits industry. Lead free solder materials, similar to the ones used herein, are generally developed by using electroplating or electroless plating options for the electronics packaging industries to eliminate toxic lead from the solder. Tin Copper and Indium Tin alloys were also successfully deposited with these methods.

[0067] Planarizer/Protective Layer Reflow Process

[0068] The wafer containing the barrier layer and the protective layer was predipped in 85 wt % H_3PO_4 and rinsed

with deionized (DI) water to remove oxidized surface material. The wafer is then rapidly heated on a hotplate with an approximate temperature of 280° C., which is well above the 75° C. indium bismuth melting point, but well below the nickel or copper melting point or the allowable 400° C. that the wafer substrate can withstand without damage to the pre-existing electrical materials/structures. The wafer was heated until the indium bismuth melted (less than 2 seconds) and then the wafer was rapidly cooled. The final structure allowed surface planarization of even very large features or surface defects, i.e. those greater than 100 μm across for 0.5μ, deep features. The final indium bismuth planarization was measured using a KLA-Tencor HRP-220 mechanical stylus profilometer. The planarization results are summarized in **FIG. 7**. Note that DoP is an abbreviation for "degree of planarization" where 1.0 is perfect planarization of a trench feature and 0.0 is no planarization. In situ reflow within the above-mentioned vacuum chamber will give improved results over conventional methods with fewer surface defects or features. Also, immediate reflow of the indium bismuth after electroplating or electroless plating deposition will give improves results over conventional methods with fewer surface defects or features.

[0069] Sacrificial Etchback of InBi to Planarize Copper Substrate/Conductive Layer

[0070] Copper, nickel and indium/bismuth pieces were etched in beakers using the following etchant combinations:

[0071] A: 4 vol % HNO_3 (70 wt %); 80 vol % H_3PO_4 (86 wt %); 16 vol % HBr (49 wt %)

[0072] B: 5 vol % HNO_3 (70 wt %); 79 vol % H_3PO_4 (86 wt %); 16 vol % HCl (37 wt %)

[0073] The etch rate results (Angstroms/min) for individual metal films are as follows for each type of etchant mix as listed above:

[0074] A: Cu=2000; Ni=1500; InBi=4200

[0075] B: Cu=2300; Ni=1800; InBi=5700

[0076] By running the etch rate tests on full-sized wafers in the tool, the across-wafer non-uniformity will be less than 5% 3-sigma for all metals. Also, by using a spin etch process on the indium/bismuth planarized wafers, the planar indium/bismuth surface will be uniformly etched at an equal rate as both the nickel and copper substrate leaving a final copper surface that is planar. Once the copper surface is planar and all sacrificial nickel and indium/bismuth is gone, then Mix A can be used to finish copper removal and polishing until stopping in the Ta on the field.

Example 2

[0077] A composition for a protective layer comprises the following components: colloidal copper oxide, copper hydrogen phosphate salts, copper acetate, copper nitrate and/or colloidal copper; and a polymeric solution of high viscosity having gelling/solidification properties suitable for functioning as the protective layer defined herein, to be used as the binder or matrix phase of the protective layer. The polymeric binder composition is an aqueous solution of high molecular weight polyethylene, polyvinyl alcohol, polyvinylpyrrolidone of such polymeric solutions doped with a solution of colloidal silica or boehmite to facilitate the formation of a rigid gel at a suitable temperature (preferably near room temperature) in the course of time and also to reduce the etch rate of the coatings to achieve nearly 1:1 selectivity with copper etching.

[0078] If the resulting etch rate of the spin-on layer, when using the standard etch solution, is greater than that of copper, the etching behavior of the standard etch solution can be altered by adding a polyethylene glycol or high molecular weight polyethylene oxide (when using a polyethylene-based protective layer). Such additives tend to lower the etch rate of the spin-on protective layer but do not change the copper etch rate, permitting an etch selectivity of 1:1 to be achieved.

[0079] In addition, the presence of phosphate-containing groups in a copper phosphate protective layer will likewise contribute to a reduction in the etch rate, when etching with etchants containing phosphoric acid.

[0080] The presence of copper salts, such as copper hydrogen phosphate, can reduce the dissolution of copper at the copper interface as the etching solution produces this type of insoluble copper phosphate. Thus, saturation of copper-containing compound at the interface will act as a chemical inhibiting layer.

Example 3

[0081] Planarizer Material/Protective Layer Deposition

[0082] A planarizer material/protective layer comprising an Accuflow material (Novalac Resin) is deposited on the conductive layer by spin track dispense. Immediately following the application of the Accuflow, the spin speed of the chuck is ramped up to create a uniform layer of Accuflow of a thickness of 1.5 um. This ramping and subsequent hot plate bakes drive off the solvent dispensed with the Accuflow as well as partially reflow the protective layer.

[0083] Planarizer/Protective Layer Cure, Reflow, and Etchback Process

[0084] The wafer containing the protective layer was cured in a furnace to drive off all remaining solvents and to complete the reflow of the Accuflow at a temperature of 350° C., well below the copper melting point or the allowable 400 C. that the wafer substrate can withstand without damage to the pre-existing electrical materials/structures. The final structure allowed surface planarization of even very large features or surface defects, i.e. those greater than 100 μm across for 0.5μ, deep features. The final Accuflow planarization was measured using a KLA-Tencor HRP-220 mechanical stylus profilometer. Once cured the Accuflow and conductor can be etched with 1:1 selectivity maintaining planarity of the surface.

[0085] Once the copper surface is planar and all sacrificial Accuflow material is gone, then Mix A can be used to finish copper removal and polishing until stopping in the Ta on the field.

Example 4

[0086] Planarizer Material/Protective Layer Deposition

[0087] A planarizer material/protective layer comprising Honeywell 512B (spin on glass material) is deposited on the conductive layer by spin track dispense. Immediately following the application of the Honeywell 512B, the spin

speed of the chuck is ramped up to create a uniform layer of 512B of a thickness of 1.0 um. This ramping and subsequent hot plate bakes drive off the solvent dispensed with the 512B as well as partially reflow the protective layer.

[0088] Planarizer/Protective Layer Cure, Reflow, and Etchback Process

[0089] The wafer containing the protective layer was cured in a furnace to drive off all remaining solvents and to complete the reflow of the 512B at a temperature of 350° C., well below the copper melting point or the allowable 400° C. that the wafer substrate can withstand without damage to the pre-existing electrical materials/structures. The final structure allowed surface planarization of even very large features or surface defects, i.e. those greater than 100 μm across for 0.5μ, deep features. The final Honeywell 512B planarization was measured using a KLA-Tencor HRP-220 mechanical stylus profilometer. Once cured the 512B and conductor can be etched with 1:1 selectivity maintaining planarity of the surface.

[0090] Once the copper surface is planar and all sacrificial Honeywell 512B is gone, then Mix A can be used to finish copper removal and polishing until stopping in the Ta on the field.

Example 5

[0091] Gallium, gallium indium, gallium alloys, and indium alloys (with near room temperature melting points), were successfully evaporatively deposited onto bare, blanket copper, patterned copper and blanket Ta coated silicon wafers. Profilometry indicated that the deposition planarized the small features on the pattern wafer.

[0092] The melted material can be spun onto the wafer using standard spin tools. The wafer will stand for a few seconds to allow the molten metal flow fill recesses and thereby planarize the wafer. Then the wafer is chilled to slightly below sub-ambient temperature (less than 20° C.) to solidify the metal planarizer. A warm solution or warm water can be used along with many common etchants (nitric acid) to remove the metal planarizer at a 1:1 selectivity with the copper from the wafer which has its sub-ambient temperature maintained by the surrounding instrumentation. The copper will require an active acid or base for its removal while a warm liquid—even warm water could be used for the metal planarizer removal while an acid (which does not attack the metal planarizer) could be used in the etching solution to remove the copper.

Example 6

[0093] The salt-like or molten salt Planarizers, such as $BiONO_3$, $B_{10}H_{14}$, $B(OH)_3$, HBO_2—alpha, beta or gamma, copper acetate, copper nitrate, $FeCl_3$, $LiClO_4$, $Mg(OH)_2$, $Mn(C_2H_3O_2)*4H_2O$, KNO_3, Ag_2CO_3, $SO_2(NH_2)_2$, $SNCl_2$, and $Zn(OH)_2$, are applied as a powder or spun on as a slurry to control thickness. The wafer is then heated in a controlled atmosphere (vacuum or inert gas) to melt the salt without damaging the existing patterned copper damascene features. The melted salt can then flow into the recessed areas, in a similar manner to the molten metals/metal planarizers listed above, thereby planarizing patterned copper features. The wafer is then cooled to re-solidify the salts into a planar film on top of the pattered copper. The etchant is then formulated to remove the copper and at the same time have the proper water and/or acid composition to remove the salt at a substantially 1:1 rate with the copper.

[0094] Thus, specific embodiments and applications of spin on planarizers and methods of production of spin on planarizers and methods of planarizing have been disclosed. It should be apparent, however, to those skilled in the art that many more modifications besides those already described are possible without departing from the inventive concepts herein. The inventive subject matter, therefore, is not to be restricted except in the spirit of the appended claims. Moreover, in interpreting both the specification and the claims, all terms should be interpreted in the broadest possible manner consistent with the context. In particular, the terms "comprises" and "comprising" should be interpreted as referring to elements, components, or steps in a non-exclusive manner, indicating that the referenced elements, components, or steps may be present, or utilized, or combined with other elements, components, or steps that are not expressly referenced.

What is claimed is:

1. An electronic component, comprising:

a substrate layer;

a dielectric material coupled to the substrate layer;

a barrier layer coupled to the dielectric material;

a conductive layer coupled to the barrier layer; and

a protective layer coupled to the conductive layer.

2. The electronic component of claim 1, wherein the dielectric material is porous and has a dielectric constant less than 3.0.

3. The electronic component of claim 1, wherein the barrier layer comprises tantalum, tantalum nitride, a stacked tantalum/tantalum nitride sandwich, or tungsten nitride (WN).

4. The electronic component of claim 1, wherein the conductive layer comprises a transition metal.

5. The electronic component of claim 4, wherein the transition metal is copper.

6. The electronic component of claim 1, wherein the protective layer comprises a viscous material.

7. The electronic component of claim 6, wherein the viscous material hardens when a curing process is applied to the viscous material.

8. The electronic component of claim 1, wherein the protective layer does not etch the conductive layer.

9. The electronic component of claim 1, wherein the protective layer comprises an organic compound, an inorganic compound, a metal material, or an inorganic metal salt.

10. A method of producing an electronic component comprising:

providing a substrate;

coupling a dielectric layer to the substrate;

coupling a barrier layer to the dielectric layer;

coupling a conductive layer to the barrier layer; and

coupling a protective layer to the conductive layer, wherein the protective layer is further planarized or acts as a planarizer.

11. The method of claim 10, wherein producing the electronic component further comprises curing the protective layer.

12. The method of claim 11, wherein curing the protective layer comprises heat curing, irradiation curing or a combination of heat curing and ashing.

13. The method of claim 11, wherein curing the protective layer comprises self-catalyzation or self-curing.

14. A method of planarizing a conductive surface of an electronic component comprising:

providing a substrate;

coupling a dielectric layer to the substrate;

coupling a barrier layer to the dielectric layer;

coupling a conductive layer to the barrier layer; and

coupling a protective layer to the conductive layer, wherein the protective layer can planarize or can be planarized.

15. The method of claim 14, wherein coupling the protective layer to the conductive layer further comprises curing the protective layer to a desirable hardness.

16. The method of claim 14, wherein introducing a protective layer onto a conductive layer comprises introducing by spin-on deposition.

17. The method of claim 14, wherein introducing a protective layer onto a conductive layer comprises introducing by electrodeposition, PVD, PECVD, CVD or vacuum evaporation.

18. The method of claim 14, wherein dispersing the protective layer across the conductive layer comprises dispersing by relative movement of the electronic component.

19. The method of claim 14, wherein curing the protective layer comprises applying heat, radiation or controlled curing.

20. The method of claim 14, wherein curing the protective layer comprises self-catalyzation.

21. The method of claim 14, wherein introducing the etching solution comprises spin etching.

22. The method of claim 14, wherein dispersing and planarizing the protective layer across the conductive layer to substantial planarity comprises etching to a degree of planarization of 1.0.

23. The method of claim 14, wherein dispersing and planarizing the protective layer across the conductive layer to substantial planarity comprises etching to a degree of planarization of 0.8.

24. The method of claim 14, wherein dispersing and planarizing the protective layer across the conductive layer to substantial planarity comprises etching to a degree of planarization of 0.6.

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(54) INTERCONNECT STRUCTURES AND A METHOD OF ELECTROLESS INTRODUCTION OF INTERCONNECT STRUCTURES

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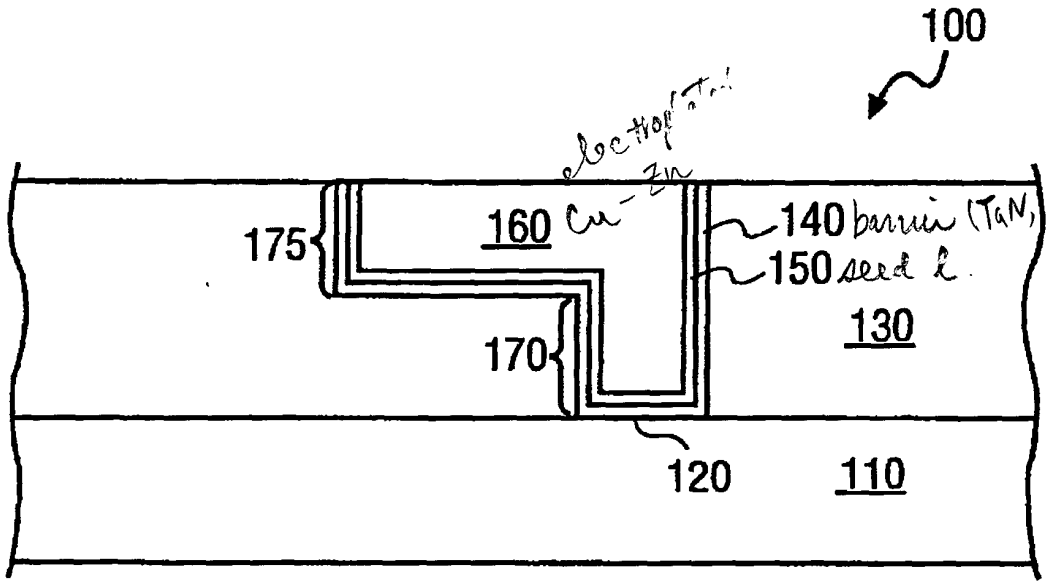
(57) **ABSTRACT**

A method comprising introducing an interconnect structure in an opening through a dielectric over a contact point, and introducing a conductive shunt material through a chemically-induced oxidation-reduction reaction. A method comprising introducing an interconnect structure in an opening through a dielectric over a contact point, introducing a conductive shunt material having an oxidation number over an exposed surface of the interconnect structure, and reducing the oxidation number of the shunt. An apparatus comprising a substrate comprising a device having contact point, a dielectric layer overlying the device with an opening to the contact point, and an interconnect structure disposed in the opening comprising an interconnect material and a different conductive shunt material.



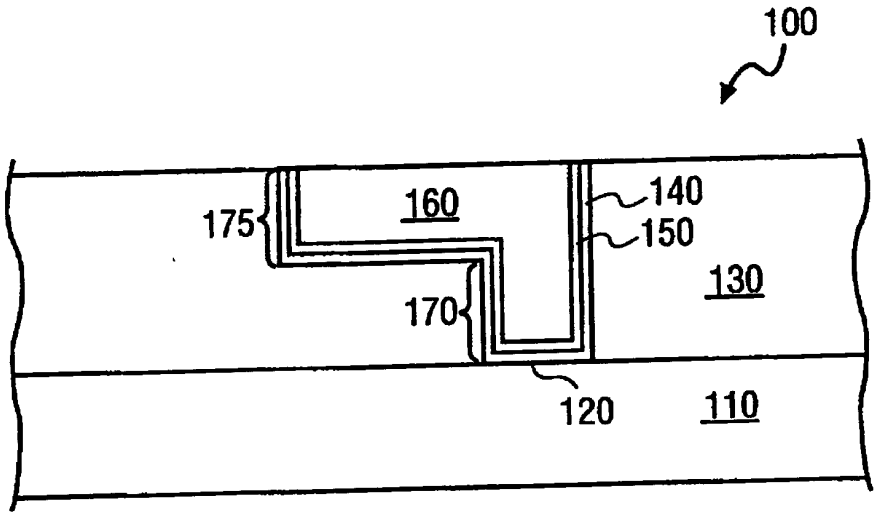

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FIG. 1

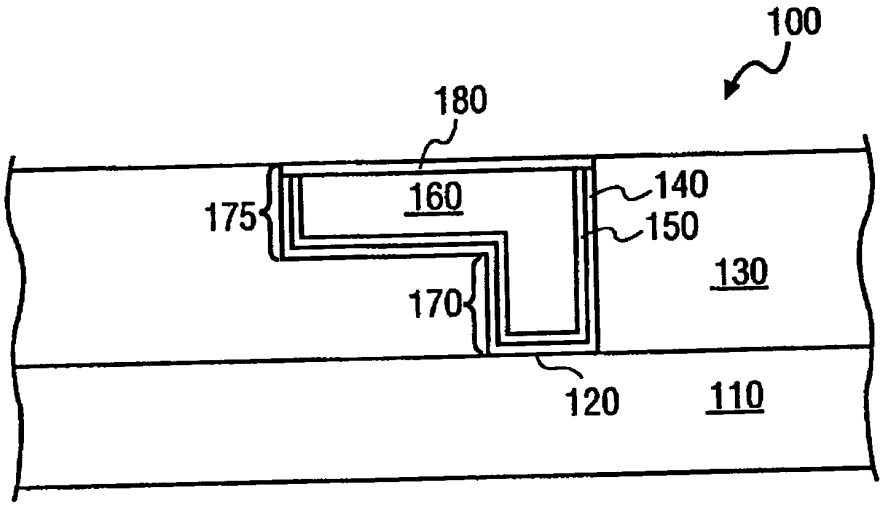
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FIG. 2

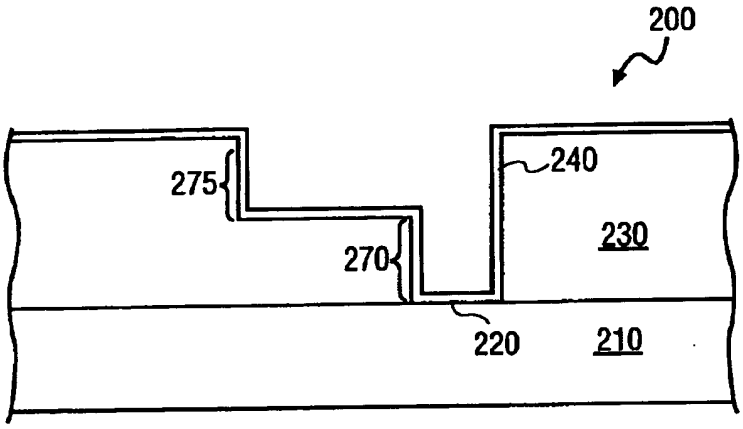

FIG. 3

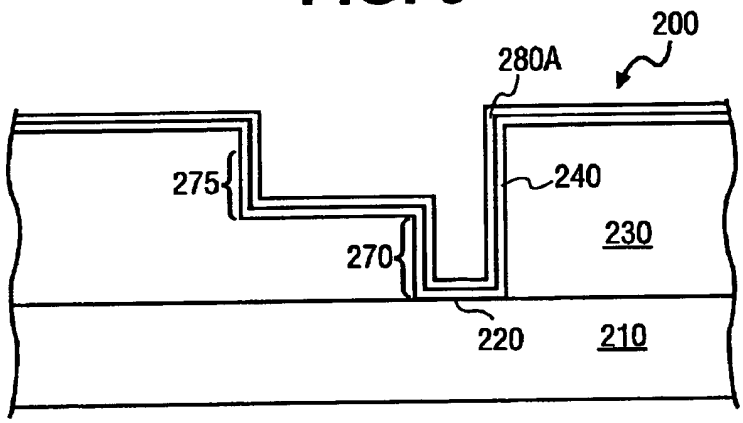

FIG. 4

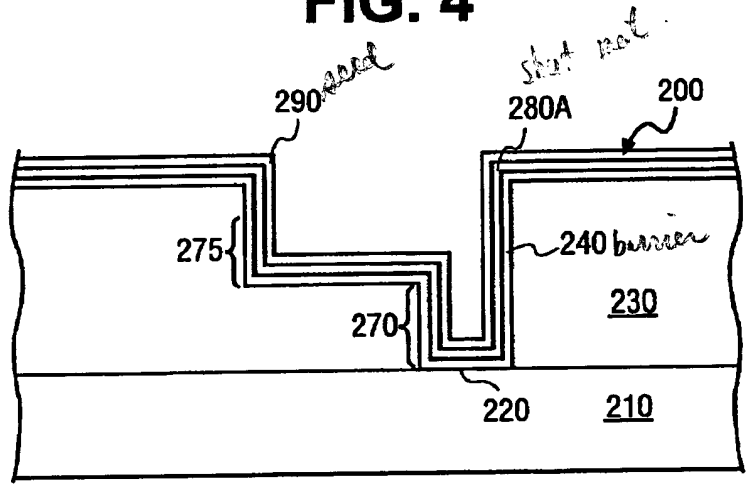

FIG. 5

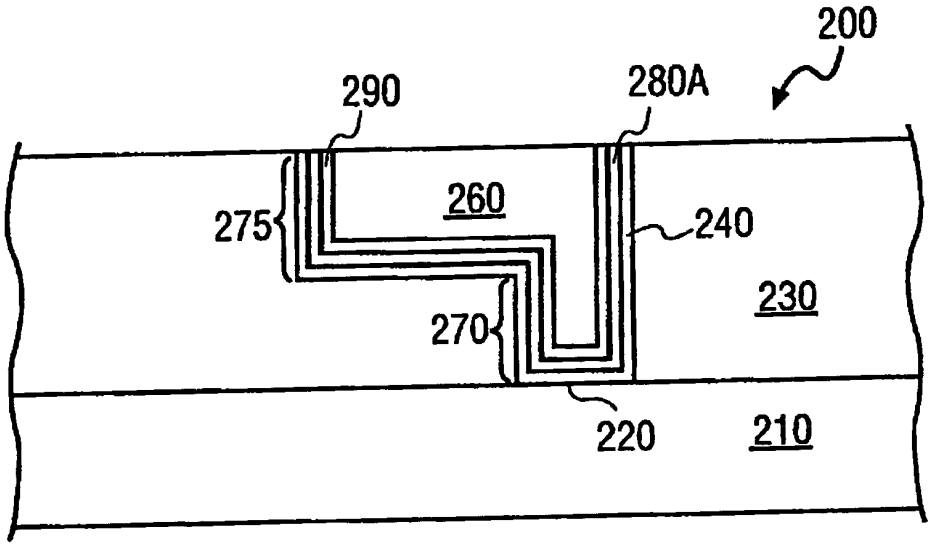
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FIG. 6

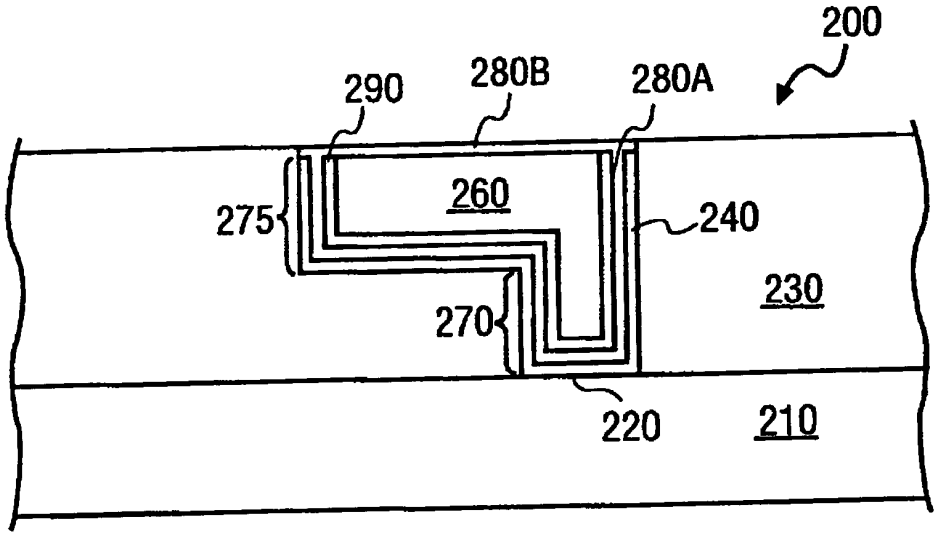
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FIG. 7

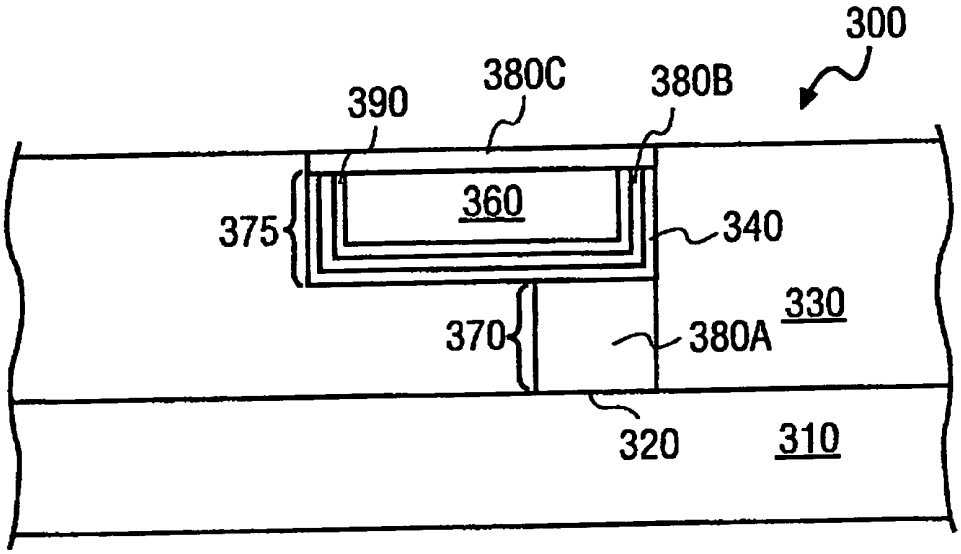

FIG. 8

INTERCONNECT STRUCTURES AND A METHOD OF ELECTROLESS INTRODUCTION OF INTERCONNECT STRUCTURES

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The invention relates to integrated circuit processing and, more particularly, to the introduction and patterning of interconnections on an integrated circuit.

[0003] 2. Description of Related Art

[0004] Modern integrated circuits use conductive interconnections to connect the individual devices on a chip or to send and/or receive signals external to the chip. Popular types of interconnections include aluminum alloy interconnections (lines) and copper interconnections (lines) coupled to individual devices, including other interconnections (lines) by interconnections through vias.

[0005] A typical method of forming an interconnection, particularly a copper interconnection, is a damascene process. A typical damascene process involves forming a via and an overlying trench in a dielectric to an underlying circuit device, such as a transistor or an interconnection. The via and trench are then lined with a barrier layer of a refractory material, such as titanium nitride (TiN), tantalum (Ta), or tantalum nitride (TaN). The barrier layer serves, in one aspect, to inhibit the diffusion of the interconnection material that will subsequently be introduced in the via and trench into the dielectric. Next, a suitable seed material is deposited on the wall or walls of the via and trench. Suitable seed materials for the deposition of copper interconnection material include copper (Cu), nickel (Ni), and cobalt (Co). Next, interconnection material, such as copper, is introduced by electroplating or physical deposition in a sufficient amount to fill the via and trench and complete the interconnect structure. Once introduced, the interconnection structure may be planarized and a dielectric material (including an interlayer dielectric material) introduced over the interconnection structure to suitably isolate the structure.

[0006] Copper has become a popular choice of interconnection material for various reasons, including its low resistivity compared with the resistivity of aluminum or aluminum alloys. Nevertheless, copper interconnection material is not without its own limitations. One limitation is that copper does not adhere well to dielectric material. The barrier material on the side walls of a via and trench as explained above provides adhesion to the adjacent dielectric material. However, in the damascene process described above, no barrier material is present on the top of the interconnect material and, consequently, copper is typically in direct contact with the dielectric material. Poor adhesion of copper material to dielectric material contributes to electromigration by the copper material during, for example, current flow.

[0007] A second problem encountered by copper interconnection material involves the difficulty in completely filling a via with copper material. In a typical electroplating introduction process, voids can appear in the via. The voids tend to aggregate and create reliability issues for the interconnection. The voids also increase the resistance of the via.

[0008] Another limitation of copper interconnection material as it is currently introduced is the tendency of the formed interconnection to blister or form hillocks due to subsequent annealing steps typically encountered in the formation of integrated circuit devices at the wafer level. These blisters or hillocks disrupt the otherwise planarized layers of interconnections over the wafer.

[0009] What is needed are improved interconnect structures and techniques for improving the introduction and properties of an interconnection structure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] **FIG. 1** shows a schematic, cross-sectional side view of an interconnect structure according to an embodiment of the invention.

[0011] **FIG. 2** shows the structure of **FIG. 1** after the introduction of a shunt material cap.

[0012] **FIG. 3** shows a schematic, cross-sectional side view of an interconnect structure formed in a dielectric material and lined with barrier material in accordance with a second embodiment of the invention.

[0013] **FIG. 4** shows the structure of **FIG. 3** after the introduction of shunt material over the barrier material.

[0014] **FIG. 5** shows the structure of **FIG. 4** after the introduction of seed material over the shunt material.

[0015] **FIG. 6** shows the structure of **FIG. 5** after the introduction of interconnect material over the seed material.

[0016] **FIG. 7** shows the structure of **FIG. 6** after the introduction of a shunt material cap.

[0017] **FIG. 8** shows a schematic, cross-sectional side view of an interconnect structure including a via substantially filled with shunt material and interconnect material encapsulated by shunt material.

DETAILED DESCRIPTION

[0018] An integrated circuit is disclosed, as well as methods for forming such a circuit. In one embodiment, an interconnect structure including a conductive shunt material is described. The shunt material may, for example, overlie the interconnection material, such as overlie copper interconnection material in a trench and via; surround the interconnection material, such as by lining the walls of a trench and via; and/or substantially fill the via of a via and trench interconnection configuration. The conductive shunt material is selected, in one aspect, for the beneficial attributes toward improving an interconnect structure. In terms of interconnect structures comprising copper, for example, such attributes include, but are not limited to, improved adhesion to dielectric material, reduction of hillocks or blistering, and reduction of electromigration.

[0019] In another embodiment, a technique for introducing a shunt material is described. That technique involves a chemically-induced oxidation-reduction reaction process described also as an electroless plating process. The electroless process allows a shunt material to be selectively introduced where desired such as on surfaces where an oxidation-reduction reaction can occur. The electroless process described herein also does not require a preliminary activation step to introduce the shunt material. Further, by controlling the components involved in the oxidation-reduction or electroless process (e.g., reducing agents, chelating

agents, pH modifiers, catalysts, etc.) the introduction of contaminant species into the interconnection material or shunt material is reduced.

[0020] **FIG. 1** shows a typical integrated circuit structure, such as a portion of a microprocessor chip on a silicon wafer. A typical integrated circuit such as a microprocessor chip may have, for example, four or five interconnection layers or levels separated from one another by dielectric material. Structure **100** includes an interconnection line over substrate **110**. Substrate **110** may be the wafer substrate having circuit devices, including transistors, thereon as well as one or more levels of interconnection to devices. **FIG. 1** shows contact point **120** that may be a circuit device formed on or in a wafer or an interconnection line formed above the wafer to devices on the wafer. It is to be appreciated that the techniques described herein may be used for various interconnections within an integrated circuit including to circuit devices and other interconnections. In this sense, contact point **120** represents such devices or interconnections where an interconnection contact is made.

[0021] **FIG. 1** illustrates a cross-sectional side view of a portion of a substrate. Overlying substrate **110** is dielectric material **130**. Dielectric material **130** is, for example, silicon dioxide (SiO_2) formed by a tetraethyl orthosilicate (TEOS) or a plasma enhanced chemical vapor deposition (PECVD) source. Dielectric material **130** may also be a material having a dielectric constant less than the dielectric constant of SiO_2 (e.g., a "low k" material), including polymers as known in the art.

[0022] **FIG. 1** shows via **170** through dielectric material **130** to expose contact point **110**. **FIG. 1** also shows trench **175** formed in a portion of dielectric material **130** over via **170**. A trench and via may be formed according to known techniques by, for example, initially using a mask, such as a photoresist mask to define an area (e.g., a cross-sectional area) for a via opening and etching the via with a suitable chemistry, such as, for example, a CH_3/CF_4 or C_4F_8 etch chemistry for SiO_2. The mask may then be removed (such as by an oxygen plasma to remove photoresist) and a second mask patterned to define a greater area (e.g., a greater cross-sectional area) for a trench opening. A subsequent mask and etch is introduced to form a trench and the second mask is removed leaving the substrate shown in **FIG. 1**.

[0023] **FIG. 1** also shows the substrate having barrier material **140** formed along the side walls of the via and trench opening. In one embodiment, barrier material **140** deposited through a thickness of approximately 10-50 nanometers (nm) depending on the desired characteristics of the barrier material. For example, barrier material **140** is chosen, in one embodiment, to be effective to inhibit interconnect material diffusion, such as copper diffusion into dielectric material **130**. Barrier material **140** may also be chosen for its adhering properties to dielectric material **130**. Suitable materials for barrier material **140** include tantalum (Ta), tantalum nitride (TaN), tantalum silicon nitride (TaSiN), tungsten (W), tungsten nitride (WN), tungsten silicon nitride (WSiN), titanium (Ti), titanium nitride (TiN), titanium silicon nitride (TiSiN), and cobalt (Co). Barrier material **140** may be introduced by conventional techniques, such as chemical vapor deposition. In one embodiment, barrier material **140** is introduced as a blanket over dielectric material **130** and along the side walls and bottom of via **170** and along the side walls of trench **175**.

[0024] Referring to **FIG. 1**, overlying barrier material **140** as a blanket including along the side walls and bottom of via **170** and trench **175** is seed material **150**. Seed material **150** is used, in one sense, in connection with a subsequent electroplating process to form an interconnection in via **170** and trench **175**. While barrier material may be a conductive material such as a titanium compound that may be capable of carrying a current utilized in an electroplating process, barrier material **140** may also not be a good conductor and may cause non-uniform current flow which, in turn, may adversely affect the electroplating process and the reliability of the interconnection. Seed material **150**, on the other hand, generally provides uniform current flow during electroplating. Moreover, seed material **150** provides enhanced adhesion of the subsequently formed interconnection to the substrate.

[0025] In one embodiment, seed material is, for example, a copper material introduced using standard chemical or physical deposition techniques. A thickness of seed material **150** along the side walls and bottom of via **170** and trench **175** of less than 3,000 angstroms (Å) is suitable.

[0026] **FIG. 1** shows structure **100** after filling via **170** and trench **175** with interconnection material **160** of, for example, a copper material. The typical introduction technique for a copper interconnection material as noted above is an electroplating process. By way of example, a typical electroplating process involves introducing a substrate (e.g., a wafer) into an aqueous solution containing metal ions, such as copper sulfate-based solution, and reducing the ions (reducing the oxidation number) to a metallic state by applying current between substrate with seed material **160** and an anode of an electroplating cell in the presence of the solution. Copper metal is deposited on to seed material **150** to fill via **170** and trench **175** and formed a copper interconnection material **160**.

[0027] In one embodiment, interconnection material **160** is copper or a copper alloy. Suitable copper alloys include copper tin (CuSn), copper-indium (CuIn), copper-cadmium (CuCd), copper-zinc (CuZn), copper-bismuth (CuBi), copper-ruthenium (CuRu), copper-rhodium (CuRh), copper-rhenium (CuRe), copper-tungsten (CuW), copper-cobalt (CuCo), copper-palladium (CuPd), copper-gold (CuAu), copper-platinum (CuPt), and copper-silver (CuAg). Alloys are generally formed by one of two methods. Typically, copper-tin, copper-indium, copper-cadmium, copper-bismuth, copper-ruthenium, copper-rhenium, copper-rhodium, and copper-tungsten are electroplated. Alternatively, copper may be doped with catalytic metals such as silver, platinum, tin, rhodium, and ruthenium by introducing a contact displacement layer on top of planarized copper interconnection material (see next paragraph) and annealing to form an alloy.

[0028] Structure **100** may be planarized such as by a chemical-mechanical polish as known in the art to dielectric material **130** to remove barrier material **140**, seed material **150**, and any interconnection material **160** present on the upper surface of dielectric material **130**. **FIG. 1** shows structure **100** having interconnect material **160**, seed material **150** and barrier material **140** introduced into via **170** and trench **175** with the surface of dielectric material **130** and the interconnect structure planarized.

[0029] **FIG. 2** shows the substrate of **FIG. 1** after the further introduction of conductive shunt material **180** to the

superior or exposed surface of the interconnect structure. Shunt material **180** is introduced, in one aspect, to improve the adhesion between interconnection material **160** and an overlying, subsequently introduced dielectric. By improving the adhesion between the interconnect structure and the subsequently introduced dielectric, the electrical migration of the interconnect structure, particularly during current flow through the interconnect structure, may be improved over prior art configurations. In a second aspect, the presence of shunt material **180** over interconnect material **160** reduces the tendency of blistering or hillock formation of interconnect material **160** due to subsequent annealing steps in the fabrication of an integrated circuit device. A further advantage of including shunt material **180** is that such material may serve as an etch stop in subsequent etching operations to the interconnect structure.

[0030] One technique for introducing shunt material **180** is through a chemically-induced oxidation-reduction reaction also referred to herein as electroless plating. Unlike an electroplating process, an electroless plating process is not accomplished by an externally-supplied current, but instead relies on the constituents of the plating process (e.g., constituents of a plating bath) to initiate and carry out the plating process. One technique involves placing structure **100** in a bath containing one or more metal ions to be plated or introduced onto the exposed conductive surfaces (e.g., conductive material **160**, seed material **150**, and barrier material **140**) as shunt material **180**; and one or more reducing agents to reduce the oxidation number of the metal ions. As described, the refractory, noble and/or transition metals are introduced in an ionic state with a positive oxidation number. Since the metals are in an ionic state having a positive oxidation number, they are in a sense shunt material precursors.

[0031] In one embodiment, the shunt material includes cobalt or nickel, or an alloy of cobalt or nickel. Suitable cobalt alloys include, but are not limited to cobalt phosphorous (CoP), cobalt-boron (CoB), cobalt-phosphorous-boron (CoPB), cobalt-metal-phosphorous (CoMeP), cobalt-metal-boron (CoMeB), and cobalt-metal-phosphorous-boron (CoMePB). As used herein, "Me" includes, but is not limited to nickel (Ni), copper (Cu), cadmium (Cd), zinc (Zn), gold (Au), silver (Ag), platinum (Pt), ruthenium (Ru), rhodium (Rh), palladium (Pd), chromium (Cr), molybdenum (Mo), iridium (Ir), rhenium (Re), and tungsten (W). The use of refractory metals (e.g., W, Re, Ru, Rh, Cr, Mo, Ir) improve the properties of shunt material **180** by improving the adhesive properties of the shunt material as well as the mechanical hardness of shunt material **180**. Combining Co and/or Ni material with a noble metal (e.g., Au, Ag, Pt, Pd, Rh, Ru) allows the noble metals to act as a catalytic surface for the electroless plating on Cu and Cu alloys lines/vias. The use of metals such as Ni, Cu, Cd, Zn, Pd, Au, Ag, Pt, Sn, Rh, and Ru allow direct introdution (e.g., deposition) of the shunt material onto barrier material. Phosphorous (P) and boron (B) are added to the shunt material as a result of reducing agent oxidation. P and B tend to improve the barrier and corrosion properties of the shunt material.

[0032] Without wishing to be bound by theory, it is believed that the exposed conductive surfaces on structure **100**, when exposed to the components of the bath, undergo an oxidation-reduction (REDOX) reaction. The oxidation number of the metal ions of the introduced shunt metal elements are reduced while the oxidation number of the reducing agent(s) are increased. Noble metals such as Au, Ag, Pt, Pd, Rh, and Ru can also displace exposed copper metal in structure **100**, the displaced copper metal being oxidized to copper ions (e.g., contact displacement). In terms of introducing metal ions of cobalt, metal ions (shunt material precursors) such as cobalt supplied by cobalt chloride, cobalt sulfate, etc., are introduced in a concentration range, in one embodiment, of about 10-70 grams per liter (g/l), alone or with the addition of compound containing metal ions of a desired alloy constituent (e.g., Ni, Cu, Cd, Zn, etc.). Examples of suitable additional compounds include ammonium tungstate (for alloying with W), ammonium perrhenate (for alloying with Re), etc. A suitable concentration range for the additional compound(s) includes 0.1 to 10 g/l.

[0033] To introduce the metal ions onto a conductive surface such as copper, tantalum or titanium, the oxidation number of the introduced metal ions is reduced. To reduce the oxidation number of the metal ions, one or more reducing agents are included in the bath. In one embodiment, the reducing agents are selected to be alkaline metal-free reducing agents such as ammonium hypophosphite, dimethylamine borate (DMAB), and/or glyoxylic acid in a concentration range of about 2 to 30 g/l. The bath may also include one or more alkaline metal-free chelating agents such as citric acid, ammonium chloride, glycine, acetic acid, and/or malonic acid in the concentration range of about 5 to 70 g/l for, in one respect, complexing copper. Still further, one or more organic additives may also be included to facilitate hydrogen evolution. Suitable organic additives include Rhodafac RE-610™, cystine, Triton x-100™, polypropylene glycol (PPG)/polyethylene glycol (PEG) (in a molecular range of approximately 200 to 10,000) in a concentration range of about 0.01 to 5 g/l. An alkaline metal-free pH adjuster such as ammonium hydroxide (NH_4OH), tetramethyl ammonium hydroxide (TMAH), tetraethyl ammonium hydroxide (TEAH), tetrapropyl ammonium hydroxide (TPAH), and/or tetrabutyl ammonium hydroxide (TBAH), may further be included in the bath to achieve a suitable pH range, such as a pH range of 3 to 14. A representative process temperature for an electroless plating bath such as described is on the order of 30 to 90° C.

[0034] By using metal-free reducing agents, additives, and pH adjusters, the plating bath contains no metals other than those desired for plating. Significantly, the plating bath, in one embodiment, does not contain potassium or sodium as typically used in prior art plating operations. Metal ions present in the bath such as potassium and sodium can contaminate a plated material. By using metal-free components, the risk of contamination is minimized. Another advantage of the described bath and the electroless process is that the plating operation may be accomplished without an activation step as previously used in typical plating processes. Still further, the use of more than one reducing agent allows various alloys to be introduced as shunt material **180**.

[0035] As described, the chemically-induced oxidation-reduction reaction or electroless plating process introduces (e.g., plates) shunt material **180** to exposed conductive surfaces (e.g., metals) amenable to a chemically-induced oxidation-reduction reaction. Prior to the plating operation, the surface of the exposed conductive material on structure **100** can be treated to improve the uniformity of the elec-

troless plating of shunt material **180**. In the case of surface treating the exposed conductive surfaces to improve uniformity of electroless shunt material plating, the exposed conductive material may be surface treated with an agent such as a 1 to 20 percent by volume hydrofluoric acid (HF), sulfuric acid (H_2SO_4), sulfonic acids such as methanesulfonic acid (MSA) ethanesulfonic acid (ESA), propanesulfonic acid (PSA), and/or benzene sulfonic acid (BSA) for cleaning of copper interconnect material.

[0036] Prior to the electroless plating process, interconnection material **160** may also be doped. In the case of doping of copper interconnection material with, for example, paladium, the doping may be accomplished by introducing a palladium activation solution. Suitable activation solutions include palladium chloride (0.01 to 2 g/l) and hydrochloric acid (0.01 to 30 milliliters per liter (ml/l)), acetic acid (100-600 ml/l), hydrofluoric acid or ammonium fluoride (1 to 70 g/l). If doping of copper lines with gold (Au), platinum (Pt), silver (Ag), tin (Sn), rhodum (Ru), and/or rutherium (Ru) is required, such metals can be introduced to the copper interconnect material by contact displacement from solutions containing the metal salts and acids such as hydrochloric acid, hydrofluoric acid, sulfuric acid, and nitric acid.

[0037] **FIG. 2** shows an interconnect structure having a shunt material as a cap or overlying structure. As a non-limiting example, a shunt material having a thickness on the order of 5 to 300 nanometers (nm) is suitable.

[0038] FIGS. **3-6** illustrate a second embodiment wherein conductive shunt material is used to encapsulate an interconnect material. Referring to **FIG. 3**, a crosssection of a portion of an integrated circuit structure similar to that described with respect to **FIG. 1** is shown. Structure **200** includes substrate **210** with contact point **220** that is a circuit device such as a transistor or an underlying interconnect structure. Via **270** and trench **275** are formed in dielectric material **230** overlying structure **210**. Barrier material **240** of, for example, tantalum, tantalum nitride, tantalum silicon nitride, tungsten, tungsten nitride, tungsten silicon nitride, titanium, titanium nitride, titanium silicon nitride, or cobalt line the side walls and bottom of via **270** and trench **275**. Optionally, a seed material (not shown) may overly barrier material **240** and via **270** and trench **275**.

[0039] **FIG. 4** shows structure **200** of **FIG. 3** after the introduction of shunt material **280A**. With reference to **FIG. 2** and the accompanying text regarding introduction of shunt material **180**, shunt material **280A** may be introduced in a similar manner by way of a chemically-induced oxidation reduction reaction or electroless plating process over the exposed conductive surfaces of structure **200**. In one embodiment, the exposed conductive surfaces of structure **200** include barrier material **240** or a seed material overlying barrier material **240** and possibly contact point **220**. Suitable materials for shunt material **280A** are similar to those described above, and include electroless metals such as cobalt and nickel, and their alloys, including alloys containing noble and refractory metals as well as metalloids such as phosphorous and boron. Referring to **FIG. 4**, shunt material **280A** lines the side walls and bottom of via **270** and trench **275**.

[0040] Following the introduction of shunt material **280A**, conformally about via **270** and trench **275**, structure **200** may be annealed to improve the adhesion of shunt material **280A** to barrier material **240**. In one embodiment, structure **200** is annealed in a reducing ambient such as nitrogen and hydrogen, hydrogen alone, or argon and hydrogen. Alternatively, structure **200** may be annealed in a vacuum.

[0041] Following the introduction of shunt material **280A** and a subsequent anneal, seed material **290** is introduced as shown in **FIG. 5** over shunt material **280A** to, in one sense, improve the adhesion between shunt material **280A** and a subsequently introduced interconnect material. A suitable seed material for a copper interconnect material is a copper-based seed. In one embodiment, a copper-based seed material may be introduced according to a electroless plating process. One way to introduce copper through an electroless plating process is submerging structure **200** in a bath containing copper ion (e.g., 1-5 g/l), EDTA (10-60 g/l), glyoxylic acid as a reducing agent (2-20 g/l), and pH adjusters such as tetramethyl ammonium hydroxide (TMAH) and/or ammonium hydroxide (NH_4OH). After the plating of electroless seed material **290**, the structure may again be annealed to improve the adhesion of seed material **290** to a subsequently introduced interconnect material. In one example, the anneal is performed in a reducing ambient (nitrogen/hydrogen, hydrogen alone, or argon/hydrogen) or a vacuum.

[0042] **FIG. 6** shows structure **200** after the introduction of interconnect material **260**. In one embodiment, interconnect material **260** is copper or a copper alloy such as described above. In the case of an alloy, as noted above, the alloy may be plated or the copper introduced and doped. Following the introduction of interconnect material **260** of, for example, copper or a copper alloy, structure **200** may be planarized, if necessary, by, for example, a chemical-mechanical polish to expose dielectric material **230** and to define the interconnect structures.

[0043] Referring to **FIG. 7**, shunt material **280B** may at this point be optionally introduced to encapsulate interconnect material **260**. Suitable materials for shunt material **280B** are similar to those described above, and include cobalt and nickel, and their alloys, including alloys containing noble and refractory metals as well as metalloids such as phosphorous and boron. The introduction of shunt material **280B** may be accomplished as described above with reference to **FIG. 2** and shunt material **180** such as by a chemically-induced oxidation-reduction reaction or electroless plating process.

[0044] Encapsulated interconnect structure, i.e., interconnect structure with encapsulated interconnect material **260** provides a mechanical frame to support interconnect material **260**. Encapsulating interconnection material **260** improves the electromigration performance particularly where dielectric material **230** is a low k dielectric material that may be softer than SiO_2. The encapsulated interconnect structure also provides an additional barrier around interconnect material **260**. In the case of copper interconnect material, it has been observed that electromigration performance is limited by surface diffusion along copper interconnect lines. By encapsulating the copper material with shunt materials **280A** and **280B**, the surface diffusion may be limited thus improving electromigration performance.

[0045] The electroless plating process described above with respect to the encapsulated structure also describes an

electroless introduction of a copper seed material. The electroless plating of seed material can replace the traditional physical deposition introduction of seed material.

[0046] In addition to the benefits noted above with respect to the encapsulated structure, the benefits seen with the shunt material cap in reference to **FIG. 2** and the accompanying text are also experienced with the encapsulated structure shown in **FIG. 7**. Namely, shunt material **280B** will improve adhesion of the interconnect structure to an overlying dielectric material, including a silicon nitride etch stop layer typically introduced as an interlayer material. Shunt material **280B** can also eliminate the need for an additional etch stop layer such as silicon nitride as shunt material **280B** can serve such purpose. In this manner, improved dielectric materials, including improved low k dielectric material may be used to isolate the interconnect structures. Still further, as noted above, shunt material **280B** will also reduce hillock or blister formation during subsequent anneal processes and will also improve the ware resistance of interconnect material **260**.

[0047] **FIG. 8** shows another embodiment of an interconnect structure. **FIG. 8** shows structure **300** that is a portion of an integrated circuit structure similar to structures **100** and **200** described above. Structure **300** includes substrate **310** having contact point **320** that is, for example, a circuit device including a transistor or an interconnect. Overlying contact point **320** is an interconnect structure formed in via **370** and trench **375** through dielectric material **330**. The interconnect structure includes shunt material **380A** introduced in via **370**. In this embodiment, shunt material **380A** substantially fills via **370**. Shunt material **380A** may be introduced by a chemically-induced oxidation-reduction reaction or electroless plating process, using contact point **320** as a surface to initiate the plating process. Alternatively, a barrier material such as described above may be introduced along the side walls and base of trench and via **370** prior to introduction of shunt material **380A**.

[0048] **FIG. 8** shows barrier material **340** introduced along the side walls and base of trench **375**. In this embodiment, barrier/seed material is omitted from the via and, instead, shunt material **380A** substantially fills via **370**. Overlying barrier material **340** is optional shunt material **380B**. Overlying shunt material **380B** is optional seed material **390** of, for example, electroless plated copper. Interconnect material **360** of, for example, copper or a copper alloy, is introduced within trench **375** to fill the trench. Shunt material **380C** is optionally introduced to encapsulate interconnect material **360** similar to the shunt material cap described above with reference to **FIG. 2**. Suitable materials for shunt material **380A**, shunt material **380B**, and shunt material **380C** are similar to those described above, and include cobalt and nickel, and their alloys, including alloys containing noble and transition metals as well as phosphorous and boron.

[0049] Advantages of selectively filling via **370** with shunt material includes that the resulting interconnect structure provides low contact resistance by eliminating an interface between plugs and metal layers where such plugs (e.g., W) may have been used in prior art processes. The introduction of shunt material **380A** in via **370**, particularly by a chemically-induced oxidation-reduction reaction or electroless plating process also reduces gap-fill problems seen in plating copper into via in the prior art. The reduction in gap-fill problems improves the vias resistance and thus the interconnect performance. While not wishing to be bound by theory, it is believed that the gap-fill problems may be avoided since the electroless process essentially glows shunt material **280A** from the surface of the underlying conductive surface, thus reducing the possibility of such via forming.

[0050] Methodologies used to introduce the above-mentioned materials and structures by electroless plating include submerging the substrate (wafer) to be plated into an electroless plating bath. Typically, the wafer is held in an apparatus with seals to prevent exposure of the backside of the wafer to plating chemicals (thereby reducing the potential for backside metal contamination of the wafer). A wafer holder may hold the wafer with the device side (where circuits are or are to be formed) face down or face up, which may reduce complications to the deposition due to gas evolution during the plating process. The temperatures required to facilitate the desired reaction may be achieved by heating the wafer, heating the bath or a combination of the two. In another embodiment, a dispensed plating is suitable. In this process, chemicals are dispensed onto the device side of the wafer while again the backside is protected from exposure. This configuration may have the advantage of limiting the interaction between reducing and oxidizing agents to tubing or other apparatus situated very close to the target wafer. Consequently, little or no depletion of the metal ions to be deposited occurs due to decomposition of the plating fluids. Again, the reaction temperatures are achieved by heating the wafer, the plating chemicals or both. In another embodiment, electroless deposition is performed on a wafer scrubber. A scrubber typically consists of cylindrical rotating pads which mechanically remove debris from both sides of the wafer. The scrubbing step is typically, the final step of a chemical mechanical polish (CMP) process. Since shunt material introduction as described above typically follows CMP, electroless introduction on a wafer scrubber allows for integration of the electroless process onto a single CMP tool.

[0051] In the preceding detailed description improved interconnect structures incorporating a shunt material and techniques of forming such structures are presented. The invention is described with reference to specific embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

What is claimed is:

1. A method comprising:

introducing a portion of an interconnect structure in an opening through a dielectric over a contact point; and

introducing a conductive shunt material adjacent the portion of the interconnect structure through a chemically-induced oxidation-reduction reaction.

2. The method of claim 1, wherein introducing the shunt material comprises introducing a shunt material precursor in the presence of a reducing agent.

3. The method of claim 2, wherein the reducing agent comprises an alkaline metal-free material.

4. The method of claim 2, wherein introducing the shunt material precursor comprises introducing the shunt material precursor in the presence of a non-metallic chelating agent.

5. The method of claim 1, further comprising:

introducing the shunt material in an alkaline environment with a pH adjusted by an alkaline metal-free pH adjuster.

6. The method of claim 1, further comprising:

prior to introducing the shunt material, modifying the exposed surface of the interconnect structure.

7. The method of claim 6, wherein modifying the surface of the interconnect structure comprises one of stripping with a stripping agent and doping with a dopant.

8. The method of claim 1, wherein introducing the interconnect structure comprises introducing a barrier material and an interconnect material, and the introduction and reduction of the shunt material precedes the introduction of the interconnect material.

9. The method of claim 8, wherein introducing the interconnect structure further includes introducing a seed material following the introduction of the barrier material.

10. The method of claim 8, wherein the opening through the dielectric material comprises a via having a cross-sectional area and a volume, and a trench to the via having a cross-sectional area greater than the cross-sectional area of the via, and introducing the shunt material comprises introducing the shunt material to substantially fill the volume of the via.

11. The method of claim 2, wherein introducing the shunt material comprises:

placing a substrate comprising the interconnect structure in a bath comprising the shunt material precursor.

12. The method of claim 11, further comprising, prior to placing the substrate in the bath, protecting a portion of the substrate to exposure to the components of the bath.

13. The method of claim 2, wherein introducing the shunt material comprises:

dispensing the shunt material precursor onto the interconnect structure.

14. The method of claim 2, wherein introducing the shunt material comprises:

placing a substrate comprising the interconnect structure in a wafer scrubber; and

while in the wafer scrubber exposing the interconnect structure to the shunt material precursor.

15. A method comprising:

introducing an interconnect structure in an opening through a dielectric over a contact point;

introducing a conductive shunt material having an oxidation number over an exposed surface of the interconnect structure; and

reducing the oxidation number of the shunt material.

16. The method of claim 15, further comprising prior to reducing the oxidation number of the shunt material, introducing a reducing agent.

17. The method of claim 16, wherein the reducing agent comprises an alkaline metal-free material.

18. The method of claim 15, further comprising:

reducing the oxidation number of the shunt material in the presence of a non-metallic chelating agent.

19. The method of claim 15, further comprising:

reducing the oxidation number of the shunt material in an alkaline environment.

20. The method of claim 15, further comprising:

prior to introducing the shunt material, modifying the exposed surface of the interconnect structure.

21. The method of claim 20, wherein modifying the surface of the interconnect comprises one of stripping with a stripping agent and doping with a dopant.

22. The method of claim 15, wherein introducing the interconnect structure comprises introducing a barrier material and an interconnect material, and the introduction and reduction of the shunt material precedes the introduction of the interconnect material.

23. The method of claim 22, wherein introducing the interconnect structure further includes introducing a seed material following the introduction of the barrier material.

24. The method of claim 22, wherein the opening through the dielectric material comprises a via having a cross-sectional area and a volume, and a trench to the via having a cross-sectional area greater than the cross-sectional area of the via, and introducing the shunt material comprises introducing the shunt material to substantially fill the volume of the via.

25. An apparatus comprising:

a substrate comprising a device having contact point;

a dielectric layer overlying the device with an opening to the contact point; and

an interconnect structure disposed in the opening comprising an interconnect material and a different conductive shunt material.

26. The apparatus of claim 25, wherein the shunt material overlies the interconnect material.

27. The apparatus of claim 26, wherein the dielectric layer is a first dielectric layer, and further comprising a second dielectric layer with an opening to the shunt material.

28. The apparatus of claim 25, wherein the interconnect structure comprises a barrier material disposed along side walls of the opening and the shunt material is disposed between the barrier material and the interconnect material.

29. The apparatus of claim 28, wherein the interconnect structure comprises a seed material and the shunt material is disposed between the seed material and the interconnect material.

30. The apparatus of claim 25, wherein the opening through the dielectric material comprises a via having a cross-sectional area and a volume, and a trench to the via having a cross-sectional area greater than the cross-sectional area of the via, and the shunt material substantially fills the volume of the via.

31. The apparatus of claim 30, wherein the interconnect structure comprises a barrier material disposed along side walls of the opening and the shunt material is disposed between the barrier material and the interconnect material.

32. The apparatus of claim 25, wherein the conductive shunt material comprises one of cobalt and a cobalt alloy.

* * * * *

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(54) METALLIZATION STRUCTURES FOR MICROELECTRONIC APPLICATIONS AND PROCESS FOR FORMING THE STRUCTURES

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(52) **U.S. Cl.** **257/586**

(57) **ABSTRACT**

A metallized structure for use in a microelectronic circuit is set forth. The metallized structure comprises a dielectric layer, an ultra-thin film bonding layer disposed exterior to the dielectric layer, and a low-Me concentration, copper-Me alloy layer disposed exterior to the ultra-thin film bonding layer. The Me is a metal other than copper and, preferably, is zinc. The concentration of the Me is less than about 5 atomic percent, preferably less than about 2 atomic percent, and even more preferably, less than about 1 atomic percent. In a preferred embodiment of the metallized structure, the dielectric layer, ultra-thin film bonding layer and the copper-Me alloy layer are all disposed immediately adjacent one another. If desired, a primary conductor, such as a film of copper, may be formed exterior to the foregoing layer sequence. The present invention also contemplates methods for forming the foregoing structure as well as electroplating baths that may be used to deposit the copper-Me alloy layer.

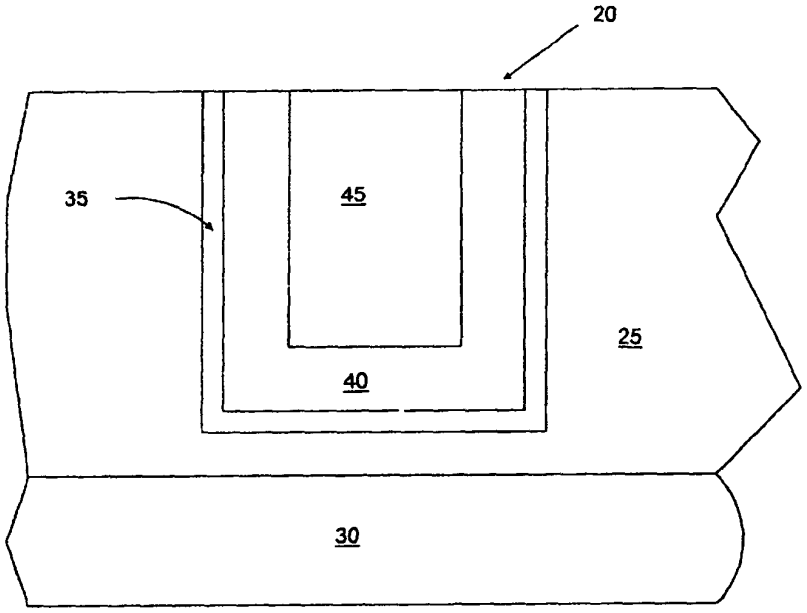
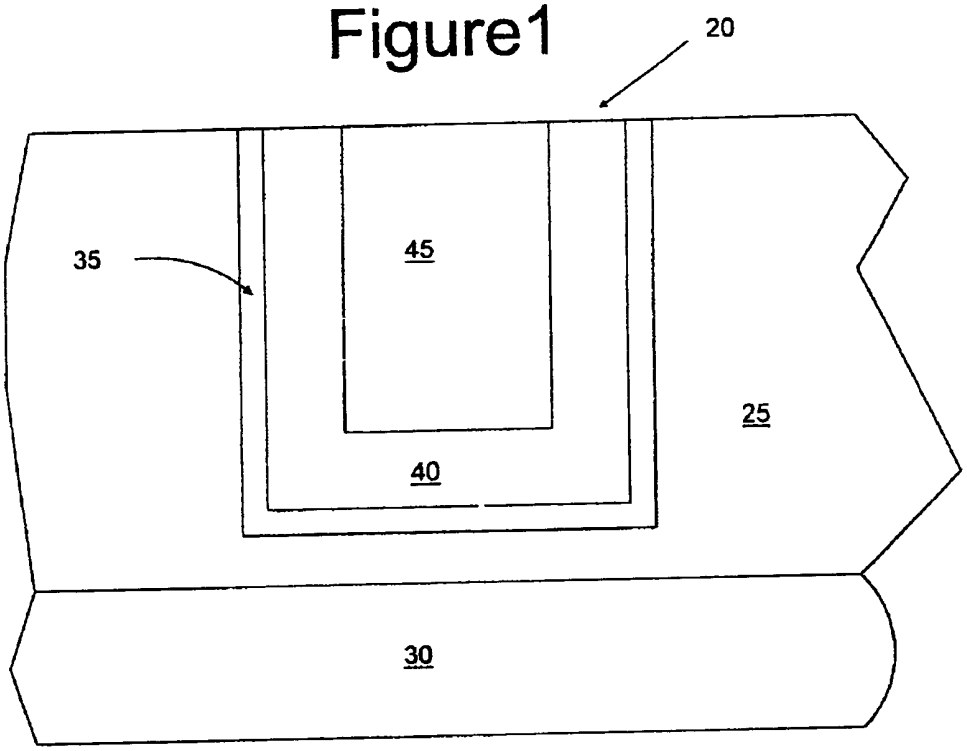


Figure1



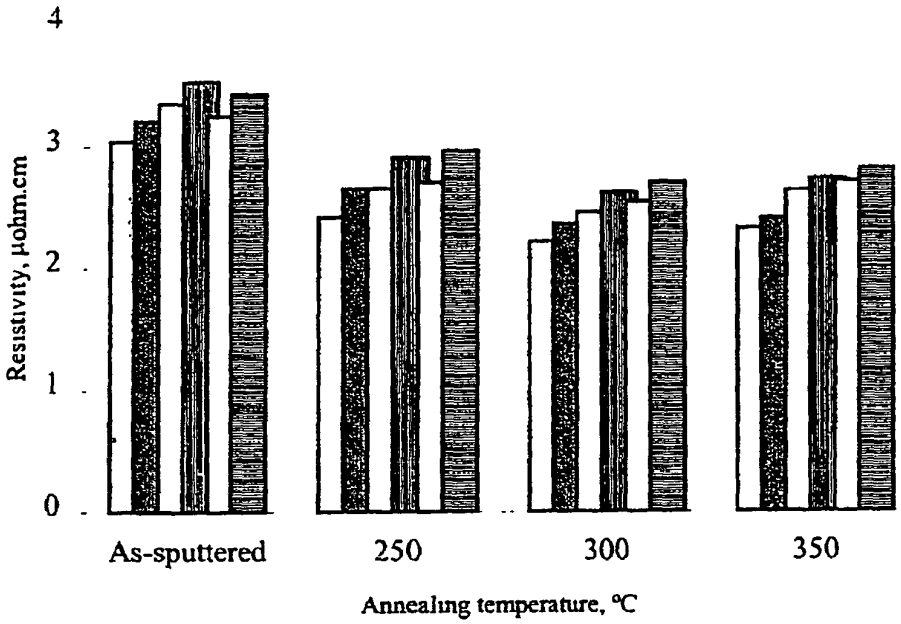

4
3
2
1
0
Resistivity, μohm.cm
As-sputtered
250
300
350
Annealing temperature, °C

FIGURE 2

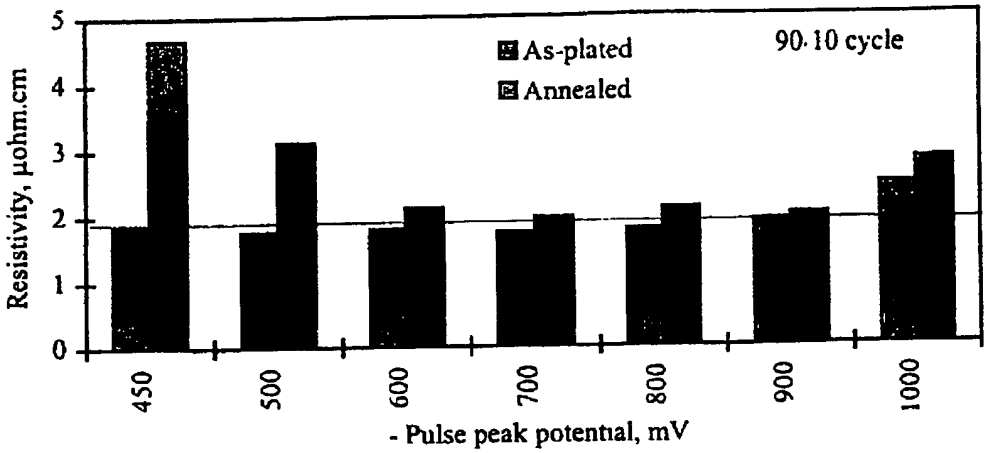


Figure 3A

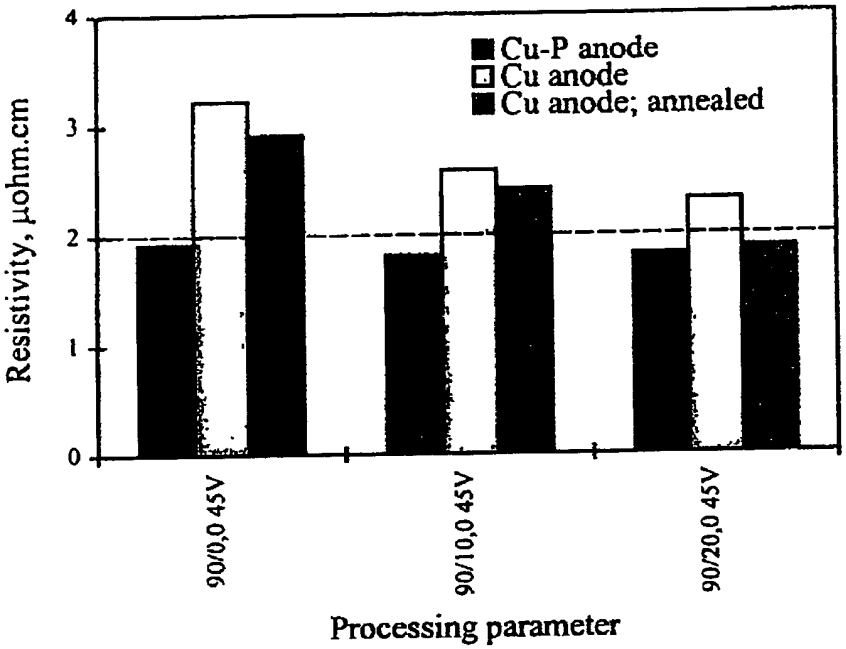


Figure 3B

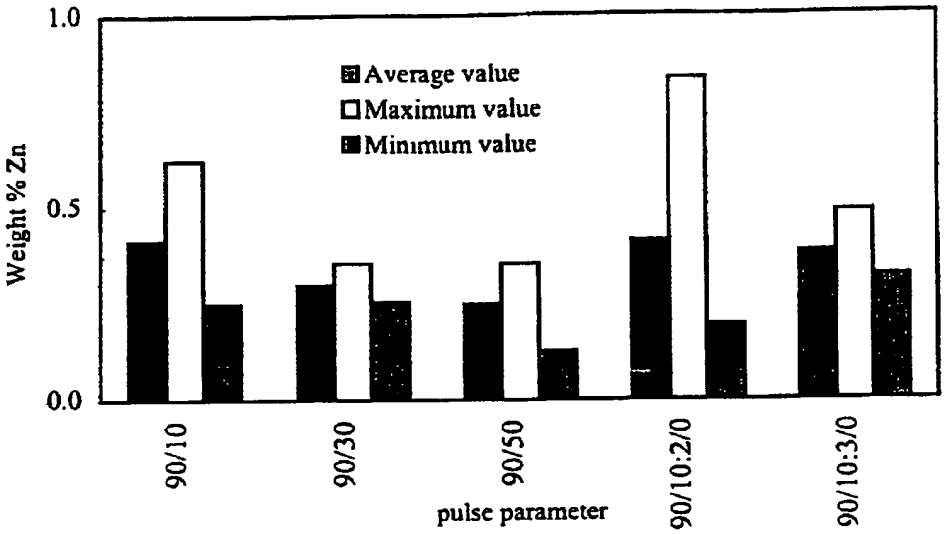

1.0
0.5
0.0
Weight % Zn
Average value
Maximum value
Minimum value
90/10
90/30
90/50
90/10:2/0
90/10:3/0
pulse parameter

Figure 4

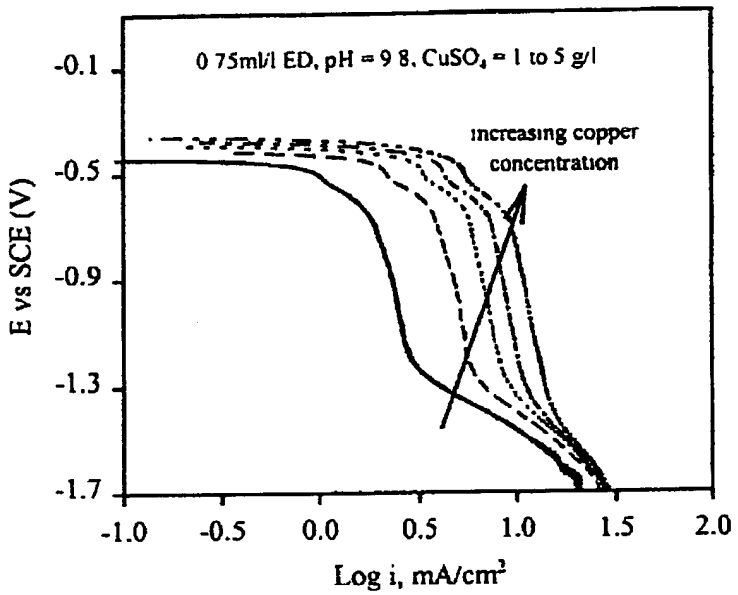


Figure 5 : Polarization curves in test solutions containing 45 g/l $ZnSO_4$ and 0 to 5 g/l $CuSO_4$

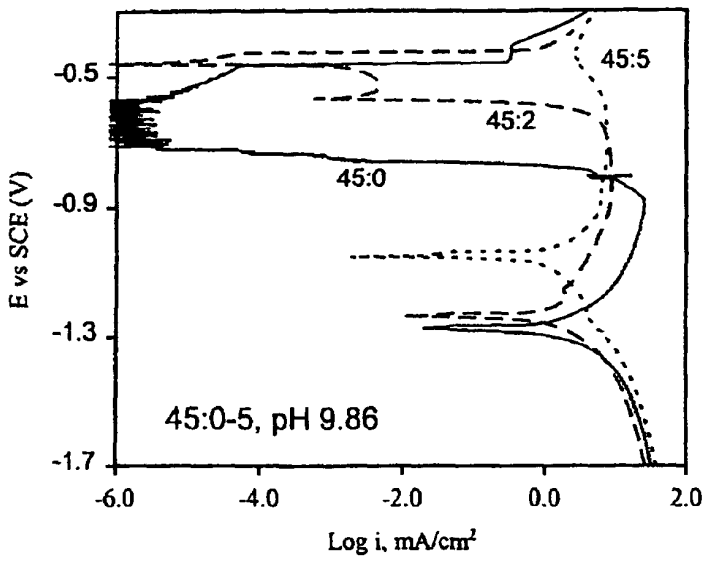


Figure 6 : Polarization curves in test solutions containing 45 g/l $ZnSO_4$ and 0 to 5 g/l $CuSO_4$

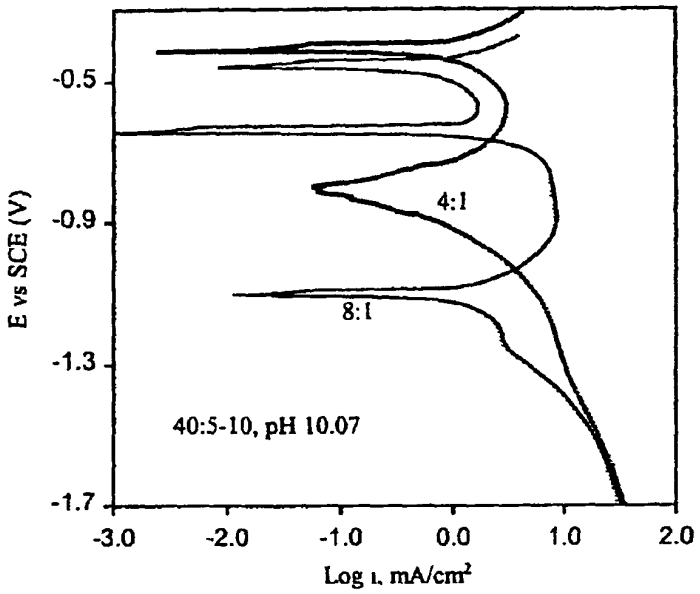


Figure 7 : Polarization curves in test solutions containing 40 g/l $ZnSO_4$ and 5 - 10 g/l $CuSO_4$

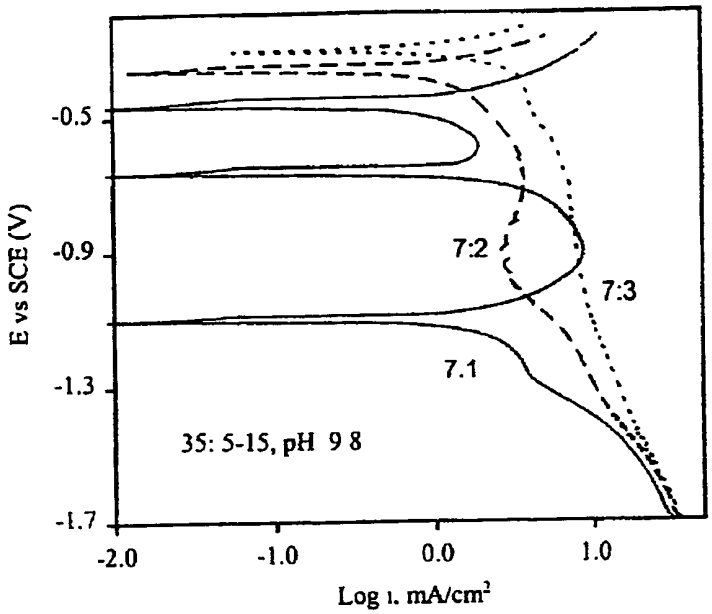


Figure 8 : Polarization curves in test solutions containing 35 g/l $ZnSO_4$ and 5 - 15 g/l $CuSO_4$

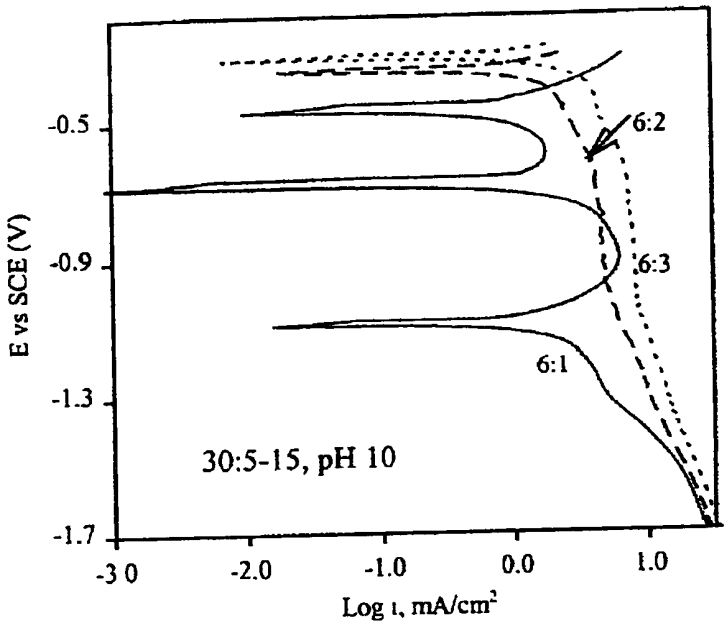


Figure 9 : Polarization curves in test solutions containing 30 g/l $ZnSO_4$ and 5 - 15 g/l $CuSO_4$

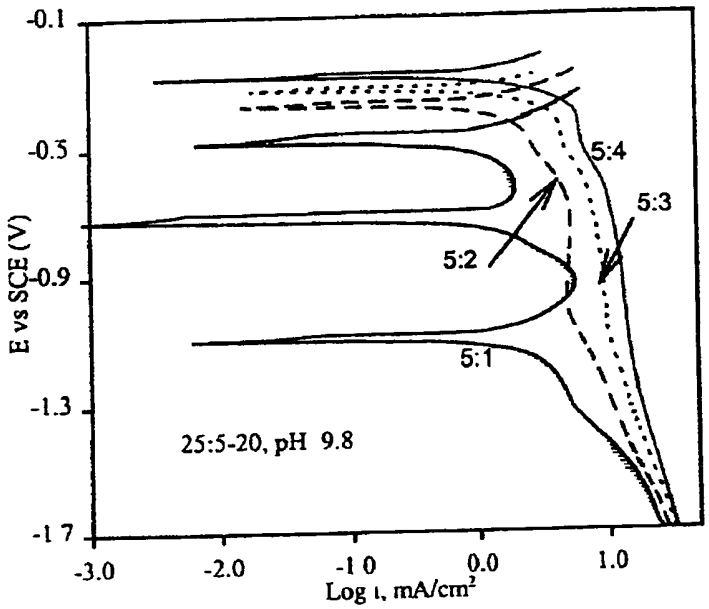


Figure 10: Polarization curves in test solutions containing 25 g/l $ZnSO_4$ and 5 - 20 g/l $CuSO_4$

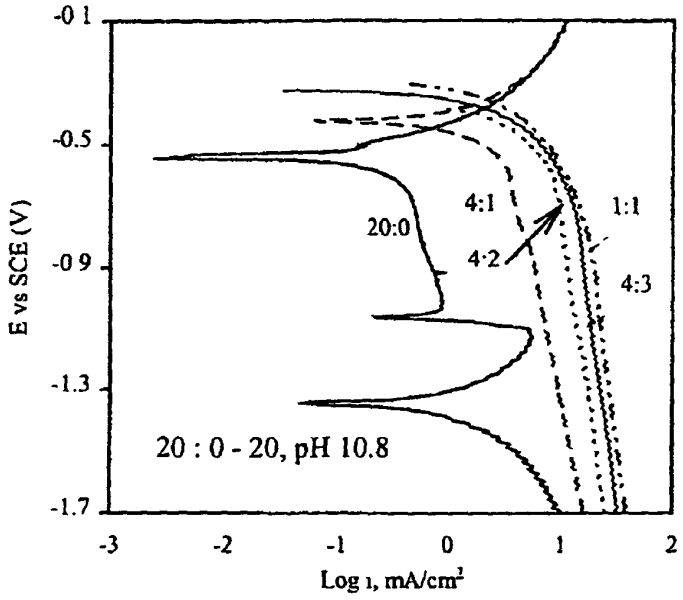


Figure 11: Polarization curves in test solutions containing 20 g/l $ZnSO_4$ and 0 - 20 g/l $CuSO_4$

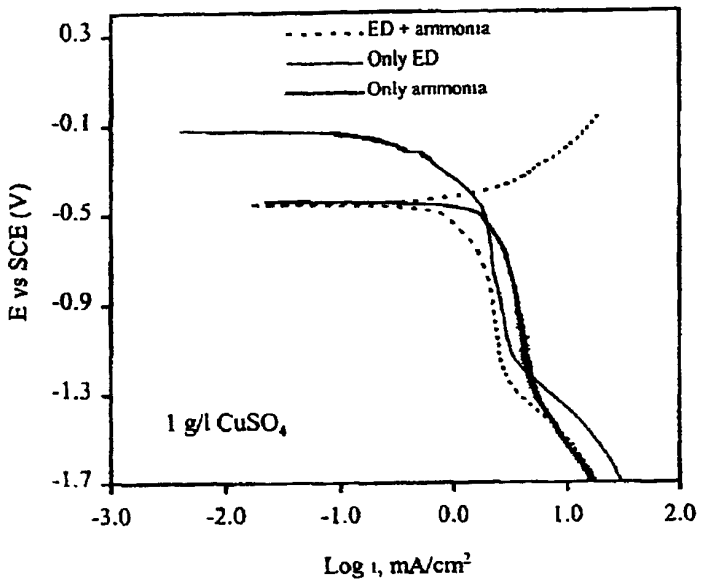


Figure 12 : Polarization curves showing the effect of ammonia and ethylene diamine

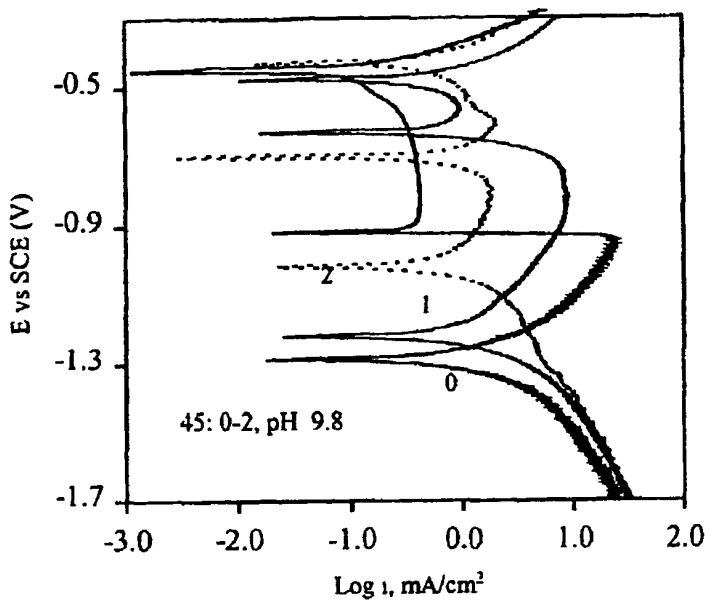


Figure 13 : Polarization curves showing the effect of addition of small quantities of copper

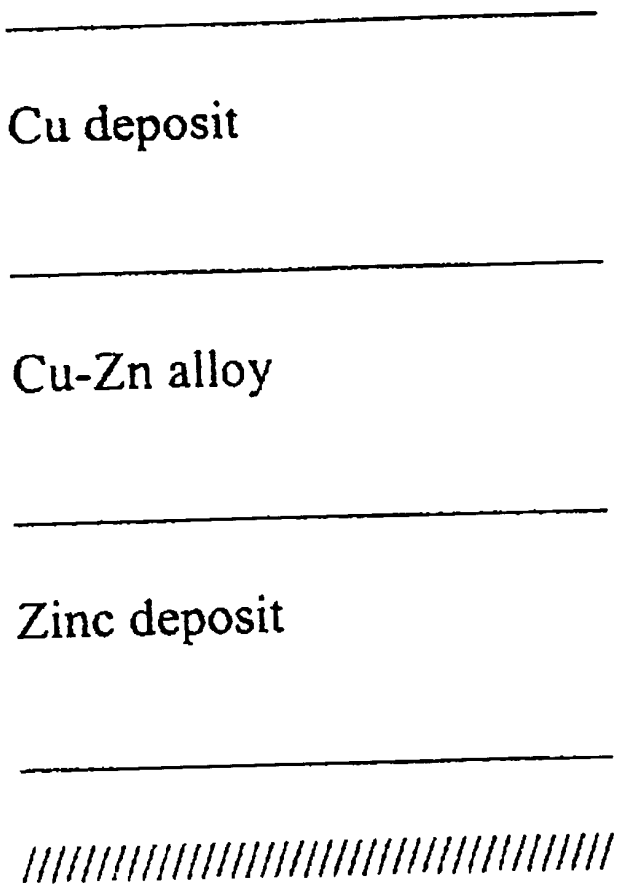


Figure 14

METALLIZATION STRUCTURES FOR MICROELECTRONIC APPLICATIONS AND PROCESS FOR FORMING THE STRUCTURES

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority from U.S. Provisional application titled "Electrochemical Co-Deposition Of A Copper-Based Alloy Metallization", Ser. No. 60/091,691, filed May 30, 1998, and from U.S. Provisional Application titled"Metallization Structures for Microelectronic Applications and Process for Forming the Structures", Ser. No. 60/114,512, filed Dec. 31, 1998.

BACKGROUND OF THE INVENTION

[0002] An integrated circuit is an interconnected ensemble of devices formed within a semiconductor material and within a dielectric material that overlies a surface of the semiconductor material. Devices which may be formed within the semiconductor material include MOS transistors, bipolar transistors, diodes and diffused resistors. Devices which may be formed within the dielectric include thin-film resistors and capacitors. Typically, more than 100 integrated circuit die (IC chips) are constructed on a single 8 inch diameter silicon wafer. The devices utilized in each dice are interconnected by conductor paths formed within the dielectric. Typically, two or more levels of conductor paths, with successive levels separated by a dielectric layer, are employed as interconnections. The metallization used to form such interconnects likewise has applicability in the formation of discrete microelectronic components, such as read/write heads, on other substrate materials. In current practice, an aluminum alloy and silicon oxide are typically used for, respectively, the conductor and dielectric.

[0003] Delays in propagation of electrical signals between devices on a single dice limit the performance of integrated circuits. Such delays in propagation also limit the performance of discrete microelectronic components. More particularly, these delays limit the speed at which an integrated circuit or microelectronic component may process or otherwise conduct these electrical signals. Larger propagation delays reduce the speed at which the integrated circuit may process the electrical signals, while smaller propagation delays increase this speed. Accordingly, integrated circuit manufacturers seek ways in which to reduce the propagation delays.

[0004] For each interconnect path, signal propagation delay may be characterized by a time delay τ. See E. H. Stevens, *Interconnect Technology,* QMC, Inc., July 1993. An approximate expression for the time delay, τ, as it relates to the transmission of a signal between transistors on an integrated circuit is given by the equation:

$$\tau=RC[1+(V_{SAT}/RI_{SAT})]$$

[0005] In this equation, R and C are, respectively, an equivalent resistance and capacitance for the interconnect path, and I_{SAT} and V_{SAT} are, respectively, the saturation (maximum) current and the drain-to-source potential at the onset of current saturation for the transistor that applies a signal to the interconnect path. The path resistance is proportional to the resistivity, ρ, of the conductor material. The path capacitance is proportional to the relative dielectric permittivity, K_e, of the dielectric material. A small value of τ requires that the interconnect line carry a current density sufficiently large to make the ratio V_{SAT}/RI_{SAT} small. It follows, therefore, that a low-ρ conductor that can carry a high current density and a low-K_e dielectric should be utilized in the manufacture of high-performance integrated circuits.

[0006] To meet the foregoing criterion, copper interconnect lines within a low-K_e dielectric will likely replace aluminum-alloy lines within a silicon oxide dielectric as the most preferred interconnect structure. See"Copper Goes Mainstream: Low-k to Follow", *Semiconductor International,* November 1997, pp. 67-70. Resistivities of copper films are in the range of 1.7 to 2.0 $\mu\Omega$cm. while resistivities of aluminum-alloy films are higher in the range of 3.0 to 3.5 $\mu\Omega$cm.

[0007] Despite the advantageous properties of copper, several problems must be addressed for copper interconnects to become viable in large-scale manufacturing processes.

[0008] Diffusion of copper is one such problem. Under the influence of an electric field, and at only moderately elevated temperatures, copper moves rapidly through silicon oxide. It is believed that copper also moves rapidly through low-K_e dielectrics. Such copper diffusion causes failure of devices formed within the silicon.

[0009] Another problem is the propensity of copper to oxidize rapidly when immersed in aqueous solutions or when exposed to an oxygen-containing atmosphere. Oxidized surfaces of the copper are rendered non-conductive and thereby limit the current carrying capability of a given conductor path when compared to a similarly dimensioned non-oxidized copper path.

[0010] A still further problem with using copper in integrated circuits is that it is difficult to use copper in a multi-layer, integrated circuit structure with dielectric materials. Using traditional methods of copper deposition, copper adheres only weakly to dielectric materials.

[0011] Finally, because copper does not form volatile halide compounds, direct plasma etching of copper cannot be employed in fine-line patterning of copper. As such, copper is difficult to use in the increasingly small geometries required for advanced integrated circuit devices.

[0012] The semiconductor industry has addressed some of the foregoing problems and has adopted a generally standard interconnect architecture for copper interconnects. To this end, the industry has found that fine-line patterning of copper can be accomplished by etching trenches and vias in a dielectric, filling the trenches and vias with a deposition of copper, and removing copper from above the top surface of the dielectric by chemical-mechanical polishing (CMP). An interconnect architecture called dual damascene can be employed to implement such an interconnect structure and thereby form copper lines within a dielectric.

[0013] At least one of the processes in the formation of the dual-damascene architecture is particularly troublesome. More particularly, deposition of thin, uniform barrier and seed layers into high aspect ratio (depth/diameter) vias and high aspect ratio (depth/width) trenches is difficult. The upper portions of such trenches and vias tend to pinch-off before the respective trench and/or via is completely filled or layered with the desired material. This problem is further

exacerbated when the interconnect structures formed in the trenches and vias include multiple layers. Conductivities of known barrier materials are negligible compared to the conductivity of copper; thus the conductance of narrow interconnect lines is markedly reduced by the barrier layer that must be interposed between the copper and dielectric.

[0014] The present inventors have found that deposition of lean alloys of copper may solve these problems. More particularly, the present inventors have determined that addition of zinc to copper in very low quantities assists in solving the diffusion and self-passivation problems and, further, have suggested a metallization structure that takes advantage of these qualities. Still further, the present inventors have developed an electroplating process that may be used to deposit the copper/zinc alloy that may be used in conjunction with the other processes employed to form the proposed metallization structure.

BRIEF SUMMARY OF THE INVENTION

[0015] A metallized structure for use in a microelectronic circuit is set forth. The metallized structure comprises a dielectric layer, an ultra-thin film bonding layer disposed exterior to the dielectric layer, and a low-Me concentration, copper-Me alloy layer disposed exterior to the ultra-thin film bonding layer. The Me is a metal other than copper and, preferably, is zinc. The concentration of the Me is less than about 5 atomic percent, preferably less than about 2 atomic percent, and even more preferably, less than about 1 atomic percent. In a preferred embodiment of the metallized structure, the dielectric layer, ultra-thin film bonding layer and the copper-Me alloy layer are all disposed immediately adjacent one another. If desired, a primary conductor, such as a film of copper, may be formed exterior to the foregoing layer sequence. The present invention also contemplates methods for forming the foregoing structure as well as electroplating baths that may be used to deposit the copper-Me alloy layer.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0016] FIG.1 illustrates a multilayer metallization structure constructed in accordance with one embodiment of the present invention.

[0017] **FIG. 2** is a chart showing the relationship between the resistivity of a copper-zinc alloy layer as a function of the annealing temperature.

[0018] **FIGS. 3A and 3B** are charts illustrating the effect of pulse parameters on the resistivity of an electrochemically deposited copper-zinc alloy layer that has been deposited using an electroplating solution having a constituent composition in accordance with one embodiment of the present invention.

[0019] **FIG. 4** is a chart illustrating the effect of pulse parameters on the zinc composition of an electrochemically deposited copper-zinc alloy that has been deposited using an electroplating solution having a constituent composition in accordance with one embodiment of the present invention.

[0020] **FIG. 5** is a graph illustrating the polarization behavior of a copper rod in copper sulfate solutions.

[0021] FIGS. 6-11 are graphs illustrating the cathodic polarization of a copper rod in plating solutions containing various quantities of zinc and copper sulfate.

[0022] **FIG. 12** is a graph illustrating the polarization response of copper in a solution containing 1 g/l of copper sulfate and others solution constituents.

[0023] **FIG. 13** is a graph illustrating polarization curves for plating solutions containing 45 g/l $ZnSO_4$ and various quantities of $CuSO_4$.

[0024] **FIG. 14** illustrates the composition of an electrochemically deposited layer that was deposited on a copper rod in tests conducted with one embodiment of the disclosed alloy electroplating solution.

DETAILED DESCRIPTION OF THE INVENTION

[0025] **FIG. 1** illustrates a multilayer metallization structure constructed in accordance with one embodiment of the present invention. As illustrated, the metallization structure, shown generally at **20**, comprises a plurality of thin layers of conductive material deposited exterior to and, preferably, directly on a dielectric layer **25**. In the specific embodiment shown here, the dielectric layer **25** is disposed exterior to and, preferably, on a substrate **30**, such as a silicori semiconductor wafer. It will be recognized that the metallization structure **20** may be disposed exterior to a wide range of thin film layer and/or substrate material types and, further, may be constructed to conform to various surface geometries. The metallization structure **20** thus has applicability to diverse classes of microelectronic components and/or interconnects.

[0026] The composition of the dielectric layer **25** is generally dependent on the function of the metallization structure **20**. When the metallization structure **20** is used to implement a post or line of an electrical interconnect network, the dielectric layer **25** is preferably comprised of a low-K material. When the metallization structure is used to implement a discrete microelectronic component such as a capacitor, however, the dielectric layer **25** is preferably comprised of a high-K material. To increase adhesion between the dielectric layer **25** and a subsequent layer, such as ultra-thin bonding layer **30**, the surface of the dielectric layer may be subject to an adhesion promoting process. For example, the dielectric surface may be subject to treatment in an atmosphere having a high ozone content. Alternatively, some form of mild mechanical or chemical abrading process may be used.

[0027] As shown in **FIG. 1**, the metallization structure **20** is comprised of an ultra-thin film bonding layer **35** disposed exterior to the dielectric layer **25**, a low-zinc concentration, copper-zinc alloy layer **40** disposed exterior to the ultra-thin film bonding layer **35**, and an optional primary conductive layer **45** disposed exterior to the copper-zinc alloy layer **40**. In a preferred embodiment illustrated here in **FIG. 1**, each of the layers **35**, **40** and **45** are immediately adjacent one another. As such, the copper-zinc alloy layer **40** is deposited directly on the bonding layer **35** and the optional primary conductive layer **45** is deposited directly on the copper-zinc alloy layer **40**.

[0028] In view of the properties of the copper-zinc alloy layer **40**, it becomes possible to use an ultra-thin bonding layer **35**. Preferably, the thickness of the bonding layer **35** is limited to a few monolayers. For example, the bonding layer thickness may be between 10-20 angstroms and, more preferably, less than about 15 angstroms.

[0029] The bonding layer **35** functions principally as an adhesion promoter to bond the copper-zinc alloy layer **40** to the dielectric layer **25**. The copper barrier characteristics of the bonding layer material are generally not as important as its bonding characteristics. This is due to the inherent self-passivation and copper-confinement properties of the copper-zinc alloy layer **40**. The present inventors have found that conducting materials that will bond with the dielectric and provide the requisite adhesion will also normally bond well with the copper of the copper-zinc alloy layer **40**. Many such materials, however, have higher resistivities than copper. Since an ultra-thin layer of the bonding material is used, however, the bonding layer **35** does not significantly contribute to the resistance of the multilayer metallization structure **20**. As such, several metals and alloys may be used as the bonding layer material. These include: Al, B, Hf. Ta, Ti, Zn, Cu, Pd, SiC, TiZn, V, Nb, Sb, Sn, nitrides, carbides, borides of refractory metals, and metallic compostructures. Generally stated, the bonding layer material may be any metal or alloy with a high magnitude free-energy of formation for the compounds that will form at the dielectric-metal interface (e.g. titanium carbide or aluminum oxide forming on a polymer/titanium interface, or silicon oxide/aluminum interface, respectively). Depending on the particular material chosen, the bonding layer **35** may be applied using one or more commonly known deposition techniques, such as PVD or CVD. As technology advances, the bonding layer **35** may ultimately be susceptible to application using an electrochemical deposition process.

[0030] The optional primary conducting layer **45** may be deposited on the copper-zinc alloy layer **40** to provide an even lower resistivity material that functions as the primary conductive path for electrical signals and, thus, reduces the overall resistance of the metallization structure **20**. The optional primary conducting layer **45** may not be necessary in situations where the copper-zinc alloy layer **40** has a resistivity that is sufficiently low to meet the circuit or component requirements. The conducting layer **45** of the illustrated embodiment, in most applications, is preferably copper. The copper layer may be deposited using any of the known film deposition techniques. However, it is preferably deposited using an electrochemical deposition technique.

[0031] One of the unique layers employed in the metallization structure **20** is the copper-zinc alloy layer **40**. The copper-zinc alloy layer **40** includes a very low zinc content. Preferably, the zinc content is below about 5 atomic percent. More preferably, the zinc content is below about 2 atomic percent. The present inventors have found that even those copper-zinc alloys having a zinc content below about 1 atomic percent exhibit properties that make them suitable for inclusion in the metallization structure **20**. A balanced approach to choosing the zinc content is generally necessary. The greater the zinc content in the alloy, the greater is the resistivity of the resulting layer. To reduce the resistivity of the alloy layer, the zinc content of the alloy should be minimized. However, with reduced zinc content, the oxidation resistance and copper-confinement properties begin to degrade. As such, the zinc content should be chosen to balance the resistivity of the layer against the oxidation resistance and copper-confinement properties. The zinc content chosen for the alloy thus becomes dependent on the performance requirements of the metallization structure **20**.

[0032] It is the properties of the copper-zinc alloy layer **40** that allow it to be used in conjunction with the very thin bonding layer **35**. By using an ultra-thin bonding layer, microstructures that are filled using the sequence of layers of metallization structure **20** include a larger proportion of high-conductivity to low-conductivity materials than can be obtained when using the thicker bonding/barrier layers that are necessary when a pure copper layer is employed without an intermediate copper-zinc alloy layer.

[0033] The copper-zinc alloy layer **40** may be deposited using sputtering techniques or, as will be set forth in greater detail below, electrochemical deposition techniques. When the layer **40** is sputter deposited, the alloy composition is generally determined by the composition of the target. Alloy layers having different zinc content are thus generally sputter deposited using different copper-zinc composition targets.

[0034] Notwithstanding the particular deposition technique used to deposit the layer, the present inventors have found that the resistivity of the copper-zinc alloy layer **40** may be reduced using a low-temperature annealing process. FIG. 2 is a chart showing the relationship between the resistivity of a copper-zinc alloy layer as a function of the annealing temperature for a number of samples in which the copper-zinc alloy was sputter deposited on the dielectric material. The sputtering was done at 2.5 kW (0.5 k volt×5 amps) with a base pressure of 10^7 Torr and an argon pressure of 5 mTorr for 10 minutes. The annealing took place at the given temperatures for a time period of 30 minutes. The sputter target had a zinc content of 5 atomic percent.

[0035] As illustrated, annealing under the foregoing conditions generally improved the resistivity of the copper-alloy layer when compared to the resistivity of the layer as originally deposited. The results show a general decrease in resistivity with increasing annealing temperature. However, the resistivity was not significantly enhanced with increasing annealing temperatures above about 350° C.-400° C. As such, given the diminishing resistivity enhancement provided above such temperatures, it has been found to be preferable to anneal the copper-zinc alloy layer at an annealing temperature that is at or below this temperature range, thereby increasing the available thermal budget of the microelectronic workpiece (e.g., a semiconductor wafer). The annealing process may take place at an even lower temperature when one or more of the layers of the overall microelectronic workpiece degrade or are otherwise stressed when subject to high annealing temperatures. For example, many low-K dielectric materials begin to degrade at temperatures above about 250 ° C.-350° C. As such, annealing must take place below such temperatures.

[0036] Although the copper-zinc alloy layer **40** may be deposited using a sputter deposition process, acid copper electroplating is becoming popular and it has a number of advantages over other types of deposition. It is relatively fast, inexpensive, easy to maintain and control, less toxic and produces deposits of good uniformity, strength and ductility. Copper and zinc, however, are widely separated in electrochemical series ($E_{Cu/Cu2+}$=+0.34 and $E_{Zn/zn2+}$=−0.76 mV with respect to Standard Hydrogen Electrode, SHE). In an acid medium, where both metals exist as simple cations, namely Cu^{2+} and Zn^{2+}, it is therefore not possible to co-deposit both copper and zinc. When an attempt is made

to electrochemically deposit two different metals having different deposition potentials from an electroplating solution, the metal having the lower magnitude deposition potential will generally plate out from the solution and a significant amount of gas will evolve before reaching the greater magnitude deposition potential of the other metal. So it therefore becomes necessary to think of chemicals, which when added to a system containing simple cations, bring the disparate deposition potentials proximate one another so that the metals can be co-deposited. To this end, complexing agents (coordinating ligands) such as cyanide, ethylenediamine, EDTA etc., may be used. These ligands coordinate with copper ions and form what are called coordinate complexes of copper thereby reducing the activity of copper and, hence, the electrode potentials. In other words, in the presence of complexing agents, the reduction potentials and, thus, the potentials at which the metals are electrodeposited, are shifted to more negative regions. The extent to which they are shifted is different for different elements. The present inventors have exploited this phenomenon to electroplate a thin film copper layer with very small amounts of zinc of less than 5 atomic percent and, more preferably, around about 1 atomic percent, and below.

[0037] To facilitate the electroplating of both copper and zinc to form the copper-zinc alloy layer **40**, a unique electroplating solution for electrochemically depositing a copper-zinc alloy was developed. The preferred solution may be used in the electrochemical deposition of the copper-zinc alloy layer **40** of the metallization structure **20** shown in **FIG. 1**, as well as in the electrochemical deposition of other copper-based alloys used for the alloy layer **40** of structure **20**. In accordance with a preferred composition of the solution, the solution includes the following constituents:

TABLE 1

PREFERRED ELECTROPLATING SOLUTION

CONSTITUENT	CONCENTRATION	FUNCTION
$MeSO_4$	10–40 g/l	Used as a source of metal, Me, that is to be alloyed with the copper (Me = zinc, aluminum, boron, magnesium, Ce, etc.)
$CuSO_4$	5–20 g/l	Used as a source of copper for the metal alloy
$(NH_4)_2SO_4$	20–40 g/l	Used as a complexing agent
Addition agent	0.1–1 ml/l	Preferably, ED or EDTA, serving as both a wetting agent as well as a complexing agent (optional constituent)
NH_4OH	50–100 ml/l	Used to adjust the pH of the solution, which should be maintained between a pH of about 8 to a pH of about 11. This constituent also functions as a complexing agent.

[0038] With the foregoing solution, it is possible to use a wide range of plating parameters to deposit a copper-zinc alloy layer **40** having a low resistivity (e.g., 1.8 –2.4 u-ohms/cm) while also having the desired oxidation resistance and copper confinement properties. Preferably, the alloy is plated using a constant potential (a. opposed to a constant current) waveform. The plating potential used is preferably between 300 mV and 900 mV cathodic. Although a DC plating waveform may be used, it is preferable to have a forward pulsed waveform. The forward pulsed waveform may have an on/off cycle of 50/20 msec to 90/10 msec. Particularly good via and trench microstructure filling results when a waveform of 0.6/0.3 msec is used.

[0039] **FIGS. 3A and 3B** are charts illustrating the effect of pulse parameters on the resistivity of the resulting copper-zinc alloy layer, while **FIG. 4** is a chart illustrating the effect of pulse parameters on the zinc composition of the resulting layer. The rightmost pulse parameter results illustrated in of each of the figures included plating waveforms having reverse pulses as well as forward pulses. As can be seen from **FIG. 4**, the zinc content of the alloy may be manipulated by varying the pulse parameters.

[0040] Although an inert anode may be used in the deposition process, a consumable anode is preferred. The consumable anode may be comprised of pure copper or of copper-phosphorous, with the copper-phosphorus anode providing better microstructure filling and better copper-alloy layer characteristics.

[0041] Various tests were performed to characterize the particular constituents used in the foregoing electroplating solution. For example, the polarization behavior of a copper rod in copper sulfate solutions is shown in **FIG. 5**. Increasing the concentration of copper in the bath shifted the SSP (Steady State Potential) to the anodic side. There did not appear to be any hydrogen evolution in the potential range studied.

[0042] The cathodic polarizations of a copper rod in plating solutions containing various quantities of zinc and copper sulfate are illustrated in FIGS. **6-11**. When the ratio of zinc to copper is in the range 8:1 to 5:1, the polarization curves go through three minima, the first one at the highest negative potential corresponds to zinc deposition/dissolution, the other two correspond to a steady state region of alloy of copper and zinc. The increase in copper content in solution shifts the curves upwards to more positive potentials. Though the ratio varies, the total amount of copper in all these examples is the same: 5 g/l. Only when the copper concentration is increased from this level to 10 g/l (in 30:10 combination, where the ratio is 3:1, but total copper sulfate concentration is 10 g/l), do the two minima at negative potentials disappear and leave only one SSP at high positive potential. This is due to the fact that the solution attains a copper dissolution/deposition equilibrium. Two parameters were thus identified: the ratio of copper sulfate to zinc sulfate in solution and the concentration of copper sulfate. Unless the copper concentration is increased above 10 g/l, it does not appear to be possible to avoid the minima at higher negative potentials. By increased addition of copper to zinc sulfate (Ratio 1:1 and copper at 20 g/l level), the current is not increased significantly. This is due to complexation, but there is an advantage of stability of the solution where the concentration decrease due to plating may not change the current density significantly. Thus it is best to utilize a composition that allows the solution to work over a wide range of potentials to obtain the same composition of the deposit.

[0043] **FIG. 12** shows the polarization response of copper in a solution containing 1 g/l copper sulfate. The presence of

ammonium hydroxide induces the formation of aminocomplexes, whereas the addition of ethylene amine induces the formation of ethylene amine complexes of metallic ions present in the solution. Whenever a complex ion is formed (by the reaction of metal ions with coordinating ligands present in solution), the activity of metal ions is reduced and this in turn reduces the deposition potential. The complexation also increases the overpotential and decreases the cathodic current density. These effects can be seen in this polarization curve. When only the amine is present, the steady state potential is around −1 V (SCE). Thus at potentials more negative to this, deposition of copper is possible. When ammonium hydroxide is present in test solution, the SSP is depressed to a higher negative value, to −0.47 V(SCE). This indicates that the complex formed with ammonia can be reduced only at higher negative potentials. The following equations represent the sequence of reactions that lead to the deposition of copper from complexes.

$$Cu^{2+}+4NH_3 \rightarrow [Cu(NH_3)_4]^{2+}$$

$$[Cu(NH_3)_4]^{2+}+2e \rightarrow Cu+NH_3$$

$$Cu_{2+}+ED \rightarrow [Cu(ED)_2]_{2+}$$

$$[Cu(ED)_2]_{2+}+2e \rightarrow Cu+2ED$$

[0044] **FIG. 13** illustrates the potentiodynamic polarization curves in plating solutions containing 45 g/l $ZnSO_4$ and various quantities of $CuSO_4$. The curves show active deposition/dissolution regions that correspond to that of zinc, copper and/or an alloy of these metals. The reduction of zinc complex to zinc occurred at potentials negative to −1.3 V (SCE) when the bath contained only zinc sulfate and no copper sulfate. The addition of 1 and 2 g/l copper sulfate resulted in this potential shifting to more anodic values, to −1.2 and −1.0 V (SCE) respectively. The steady state region that corresponds to that of pure zinc was masked by the simultaneous copper deposition. The extent to which this occurred depended on the amount of copper in the bath. Thus even before zinc that deposited at higher potentials dissolved, copper/copper alloy started to deposit. To observe the cross section of the cathodically polarized specimens, the experiment was terminated when the current in the cathodic region went below 100 μA (approximately at −0.5 V SCE). The specimen was then polished to observe the layers from surface to inside. As illustrated in **FIG. 14**, the layers were seen to be copper, Cu—Zn alloy and zinc as viewed from from the deposit surface to copper rod/deposit interface.

[0045] The electrochemical deposition of the copper-zinc alloy layer **40** may be implemented in a wide range of electroplating reactor types. An integrated processing tool that incorporates one or more electroplating reactors that are particularly suitable for implementing the foregoing electrochemical deposition process is available from Semitool, Inc., of Kalispell, Montana. Such tools are sold under the brand names LT-210™ and Equinox™ and are readily adapted to implement a wide range of electroplating processes used in the fabrication of microelectronic circuits and components. Advantageously, the reactors employed in these tools rotate a workpiece during the electrochemical deposition process, thereby enhancing the uniformity of the resulting film. It is preferable to rotate a workpiece when depositing the copper-zinc alloy layer **40** (or other alloy layer) onto the workpiece. To further enhance the quality of the resulting copper-Zn alloy layer **40**, the electrochemical deposition reaction chamber(s) of these tools may be fitted with an ultrasonic generator that provides ultrasonic energy to the electroplating solution during the electrochemical deposition process to hereby enhance the desired characteristics of the resulting alloy layer.

[0046] In addition to electroplating reactors, such tools frequently include other ancillary processing chambers such as, for example, pre-wetting chambers, rinsing chambers, etc., that are used to perform other processes typically associated with electrochemical deposition. Semiconductor wafers, as well as other microelectronic workpieces, are processed in such tools one-by-one in the reactors and are transferred between the processing stations, as well as between the processing stations and input/output stations, by a robotic transfer mechanism. The robotic transfer mechanism, the electroplating reactors and the plating recipes used therein, as well as the components of the processing chambers are all under the control of one or more programmable processing units.

[0047] Numerous modifications may be made to the foregoing inventions without departing from the basic teachings thereof. Although the present inventions have been described in substantial detail with reference to one or more specific embodiments, those of skill in the art will recognize that changes may be made thereto without departing from the scope and spirit of the invention as set forth in the appended claims.

What is claimed is:

1. A metallized structure for use in a microelectronic circuit, the metallized structure comprising:

a dielectric layer;

an ultra-thin film bonding layer disposed exterior to the dielectric layer; and

a low-Me concentration, copper-Me alloy layer disposed exterior to the ultra-thin film bonding layer.

2. A metallized structure as set forth in claim 1 wherein the dielectric layer is formed from a low-K dielectric material.

3. A metallized structure as set forth in claim 1 wherein the dielectric layer is formed from a high-K dielectric material.

4. A metallized structure as set forth in claim 1 wherein the Me content of the copper-Me alloy layer is less than or equal to about 5 atomic percent.

5. A metallized structure as set forth in claim 1 wherein the zinc content of the copper-Me alloy layer is less than or equal to about 2 atomic percent.

6. A metallized structure as set forth in claim 1 wherein the zinc content of the copper-Me alloy layer is less than or equal to about 1 atomic percent.

7. A metallized structure as set forth in claim 1 wherein the ultra-thin bonding layer has a thickness between about 10-20 angstrom s.

8. A metallized structure as set forth in claim 7 wherein the ultra-thin bonding layer has a thickness of less than about 15 angstroms.

9. A metallized structure as set forth in claim 1 wherein the ultra-thin bonding layer is comprised of a metal.

10. A metallized structure as set forth in claim 1 wherein the ultra-thin bonding layer is comprised of a metal alloy.

11. A metallized structure for use in a microelectronic circuit, the metallized structure comprising:

a dielectric layer;

an ultra-thin film bonding layer disposed exterior to the dielectric layer; and

a low-zinc concentration, copper-zinc alloy layer disposed exterior to the ultra-thin film bonding layer.

12. A metallized structure as set forth in claim 11 and further comprising a primary copper conductor disposed exterior to the low-zinc concentration, copper-zinc alloy layer.

13. A metallized structure as set forth in claim 11 wherein the dielectric layer is formed from a low-K dielectric material.

14. A metallized structure as set forth in claim 11 wherein the dielectric layer is formed from a high-K dielectric material.

15. A metallized structure as set forth in claim 11 wherein the zinc content of the copper-zinc alloy layer is less than or equal to about 5 atomic percent.

16. A metallized structure as set forth in claim 11 wherein the zinc content of the copper-zinc alloy layer is less than or equal to about 2 atomic percent.

17. A metallized structure as set forth in claim 11 wherein the zinc content of the copper-zinc alloy layer is less than or equal to about 1 atomic percent.

18. A metallized structure as set forth in claim 11 wherein the ultra-thin bonding layer has a thickness between about 10-20 angstroms.

19. A metallized structure as set forth in claim 18 wherein the ultra-thin bonding layer has a thickness of less than about 15 angstroms.

20. A metallized structure as set forth in claim 11 wherein the ultra-thin bonding layer is comprised of a metal.

21. A metallized structure as set forth in claim 11 wherein the ultra-thin bonding layer is comprised of a metal alloy.

22. A metallized structure for use in a microelectronic circuit, the metallized structure comprising:

a dielectric layer;

an ultra-thin film bonding layer disposed adjacent to the dielectric layer; and

a low-zinc concentration, copper-zinc alloy layer disposed adjacent to the ultra-thin film bonding layer.

23. A metallized structure as set forth in claim 22 and further comprising a primary copper conductor layer adjacent the low-zinc concentration, copper-zinc alloy layer.

24. A metallized structure as set forth in claim 22 wherein the dielectric layer is formed from a low-K dielectric material.

25. A metallized structure as set forth in claim 22 wherein the dielectric layer is formed from a high-K dielectric material.

26. A metallized structure as set forth in claim 22 wherein the zinc content of the copper-zinc alloy layer is less than or equal to about 5 atomic percent.

27. A metallized structure as set forth in claim 22 wherein the zinc content of the copper-zinc alloy layer is less than or equal to about 2 atomic percent.

28. A metallized structure as set forth in claim 22 wherein the zinc content of the copper-zinc alloy layer is less than or equal to about 1 atomic percent.

29. A metallized structure as set forth in claim 22 wherein the ultra-thin bonding layer has a thickness between about 10-20 angstroms.

30. A metallized structure as set forth in claim 29 wherein the ultra-thin bonding layer has a thickness of less than about 15 angstroms.

31. A metallized structure as set forth in claim 22 wherein the ultra-thin bonding layer is formed from a material with a high magnitude free-energy of formation for compounds that will form at the dielectric-bonding layer interface.

32. A metallized structure as set forth in claim 22 wherein the ultra-thin bonding layer is comprised of a metal.

33. A metallized structure as set forth in claim 22 wherein the ultra-thin bonding layer is comprised of a metal alloy.

34. A method for forming a metallized structure on a microelectronic workpiece comprising the steps of:

depositing a dielectric layer on the microelectronic workpiece;

depositing an ultra-thin bonding layer exterior to the dielectric layer;

depositing a low Me concentration, copper-Me alloy layer exterior to the ultra-thin bonding layer, where Me is a metal other than copper.

35. A method for forming a metallized structure as set forth in claim 34 wherein the ultra-thin bonding layer is disposed immediately adjacent the dielectric layer and the copper-Me alloy layer is disposed immediately adjacent the ultra-thin bonding layer.

36. A method for forming a metallized structure as set forth in claim 35 wherein the concentration of Me is less than about 5 atomic percent.

37. A method for forming a metallized structure as set forth in claim 35 wherein the concentration of Me is less than about 2 atomic percent.

38. A method for forming a metallized structure as set forth in claim 35 wherein the concentration of Me is less than about 1 atomic percent.

39. A method for forming a metallized structure as set forth in claim 35 wherein Me is zinc.

40. A method for forming a metallized structure as set forth in claim 36 wherein Me is zinc.

41. A method for forming a metallized structure in set forth in claim 37 wherein Me is zinc.

42. A method for forming a metallized structure in set forth in claim 38 wherein Me is zinc.

43. A method for forming a metallized structure as set forth in claim 34 wherein the copper-Me alloy layer is deposited using an electrochemical deposition process.

44. A method for forming a metallized structure as set forth in claim 43 wherein the electrochemical deposition process uses a constant potential waveform.

45. A method for forming a metallized structure as set forth in claim 44 wherein the constant potential waveform comprises a forward pulsed waveform.

46. A method for forming a metallized structure as set forth in claim 35 wherein the copper-Me alloy layer is deposited using an electrochemical deposition process.

47. A method for forming a metallized structure as set forth in claim 41 wherein the copper-Me alloy layer is deposited using an electrochemical deposition process.

48. An electroplating bath for depositing a low-Me concentration, copper-Me alloy layer on the surface of a microelectronic workpiece, where Me is a metal other than copper, the bath comprising:

$MeSO_4$ as a source of the metal Me;

$CuSO_4$ as a source of copper;

$(NH_4)_2SO_4$ as a complexing agent; and

NH_4OH as a pH adjuster.

49. An electroplating bath as set forth in claim 48 wherein the $MeSO_4$ is $ZnSO_4$.

50. An electroplating bath as set forth in claim 48 wherein Me in the $MeSO_4$ is selected from the group consisting of the zinc, aluminum, boron, magnesium, and cesium.

51. An electroplating bath as set forth in claim 48 and further comprising an addition agent that serves as both a wetting agent and a complexing agent.

52. An electroplating bath as set forth in claim 51 wherein the addition agent is a chemical selected from the group consisting of ED and EDTA.

53. An electroplating bath for depositing a low-Me concentration, copper-Me alloy layer on the surface of a microelectronic workpiece, where Me is a metal other than copper, the bath comprising:

$MeSO_4$ as a source of the metal Me, the $MeSO_4$ being in the electroplating bath at a concentration between about 10-40 g/l;

$CuSO_4$ as a source of copper, the $CuSO_4$ being in the electroplating bath at a concentration between about 5-20 g/l;

$(NH_4)_2SO_4$ as a complexing agent, the $(NH_4)_2SO_4$ being in the electroplating bath at a concentration between about 20-40 g/l ; and

NH_4 OH as a pH adjuster, the $(NH_4)_2SO_4$ being in the electroplating bath at a concentration between about 50-100 g/l.

54. An electroplating bath as set forth in claim 53 wherein the $MeSO_4$ is $ZnSO_4$.

55. An electroplating bath as set forth in claim 53 wherein Me in the $MeSO_4$ is selected from the group consisting of the zinc, aluminum, boron, magnesium, and cesium.

56. An electroplating bath as set forth in claim 53 and further comprising an addition agent that serves as both a wetting agent and a complexing agent.

57. An electroplating bath as set forth in claim 56 wherein the addition agent is a chemical selected from the group consisting of ED and EDTA.

58. An electroplating bath as set forth in claim 57 wherein the addition agent is present in the electroplating bath at a concentration that is between about 0.1-1 ml/l.

59. An electroplating bath as set forth in claim 53 wherein the pH of the electroplating bath is about 11.

* * * * *

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Chen (43) **Pub. Date: Nov. 22, 2001**

(54) **APPARATUS AND METHOD FOR ELECTROLYTICALLY DEPOSITING COPPER ON A SEMICONDUCTOR WORKPIECE**

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(21) Appl. No.: **09/885,232**

(22) Filed: **Jun. 20, 2001**

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(52) **U.S. Cl.** **205/108**; 205/118; 205/291; 205/295; 205/170; 205/182; 205/183

(57) **ABSTRACT**

This invention employs a novel approach to the copper metallization of a workpiece, such as a semiconductor workpiece. In accordance with the invention, an alkaline electrolytic copper bath is used to electroplate copper onto a seed layer, electroplate copper directly onto a barrier layer material, or enhance an ultra-thin copper seed layer which has been deposited on the barrier layer using a deposition process such as PVD. The resulting copper layer provides an excellent conformal copper coating that fills trenches, vias, and other microstructures in the workpiece. When used for seed layer enhancement, the resulting copper seed layer provide an excellent conformal copper coating that allows the microstructures to be filled with a copper layer having good uniformity using electrochemical deposition techniques. Further, copper layers that are electroplated in the disclosed manner exhibit low sheet resistance and are readily annealed at low temperatures.

Fig. 1

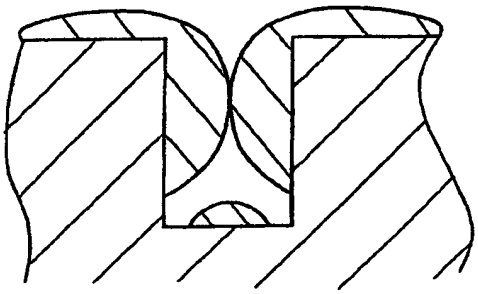


Fig. 2A

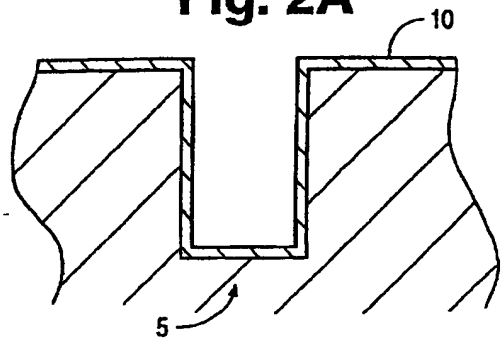


Fig. 2B

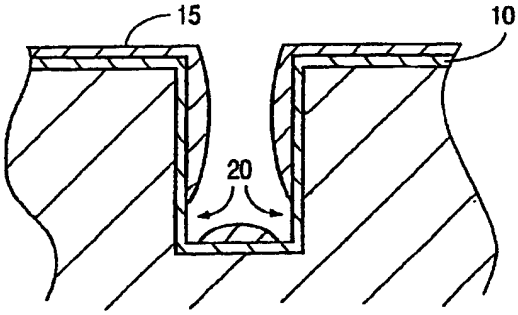


Fig. 2C

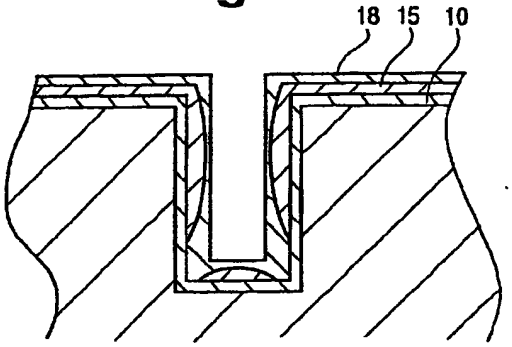


Fig. 2D

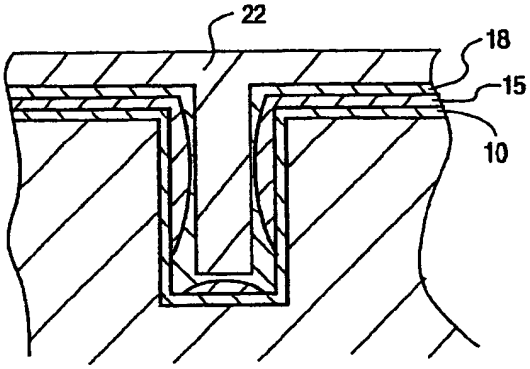


Fig. 2E

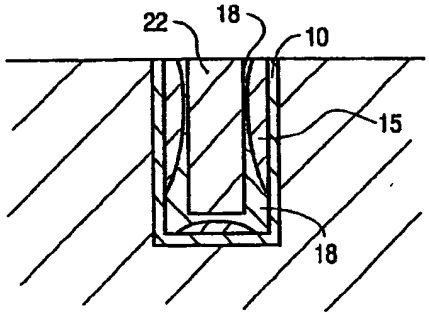
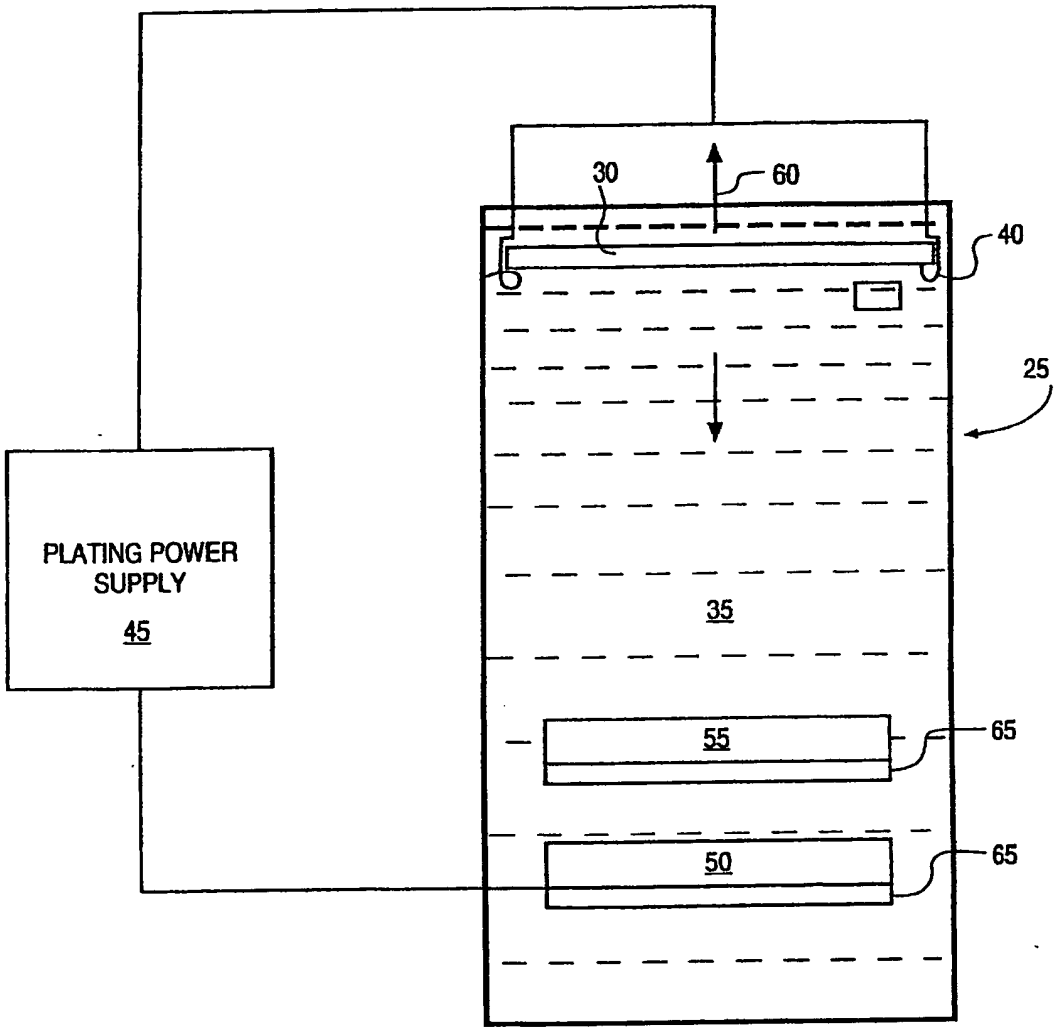


Fig. 3



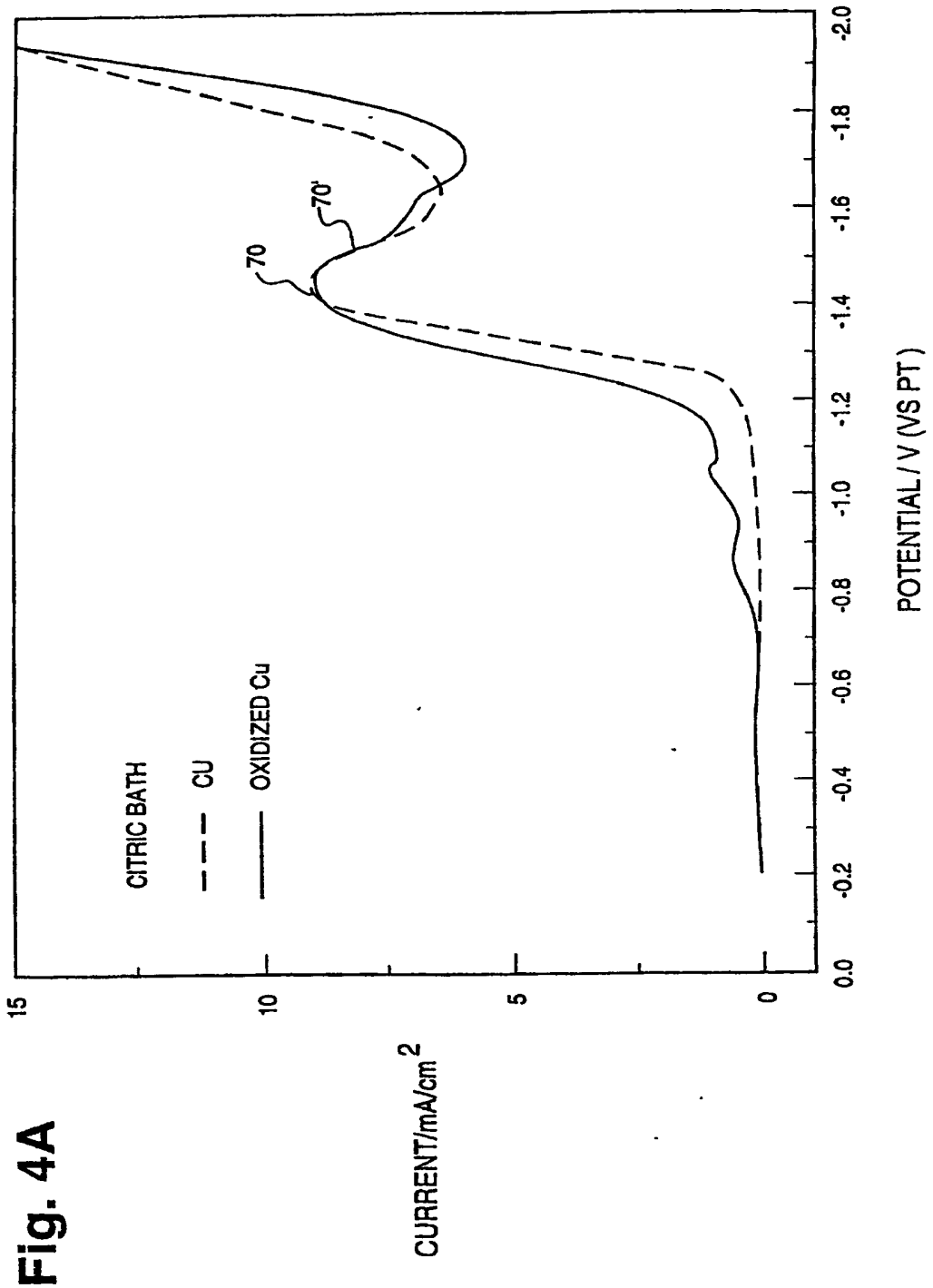

CITRIC BATH
CU
OXIDIZED Cu
70
70'
15
10
5
0
CURRENT/mA/cm2
0.0
-0.2
-0.4
-0.6
-0.8
-1.0
-1.2
-1.4
-1.6
-1.8
-2.0
POTENTIAL / V (VS PT)

Fig. 4A

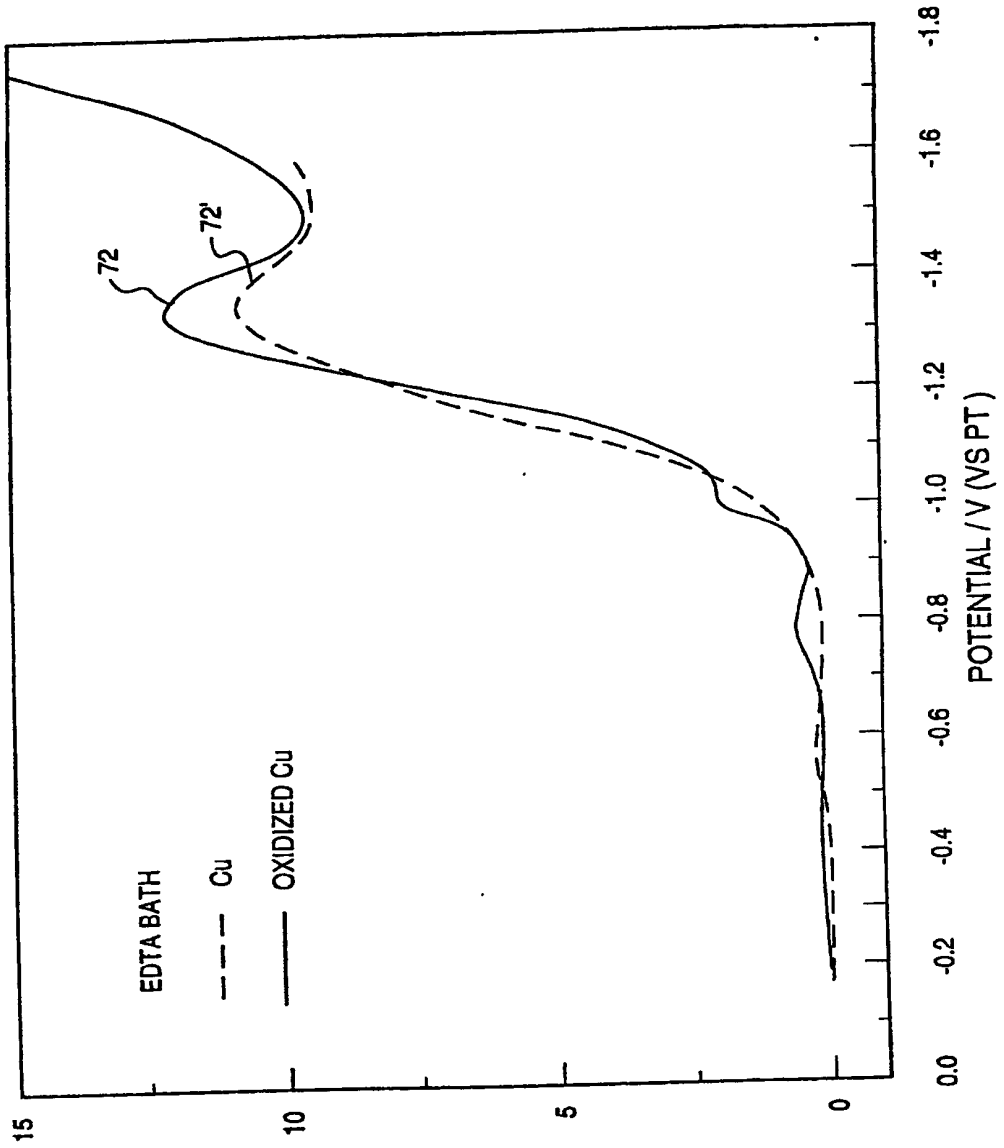

72
72'
EDTA BATH
Cu
OXIDIZED Cu
CURRENT/mA/cm^2
15
10
5
0
0.0
-0.2
-0.4
-0.6
-0.8
-1.0
-1.2
-1.4
-1.6
-1.8
POTENTIAL / V (VS PT)

Fig. 4B

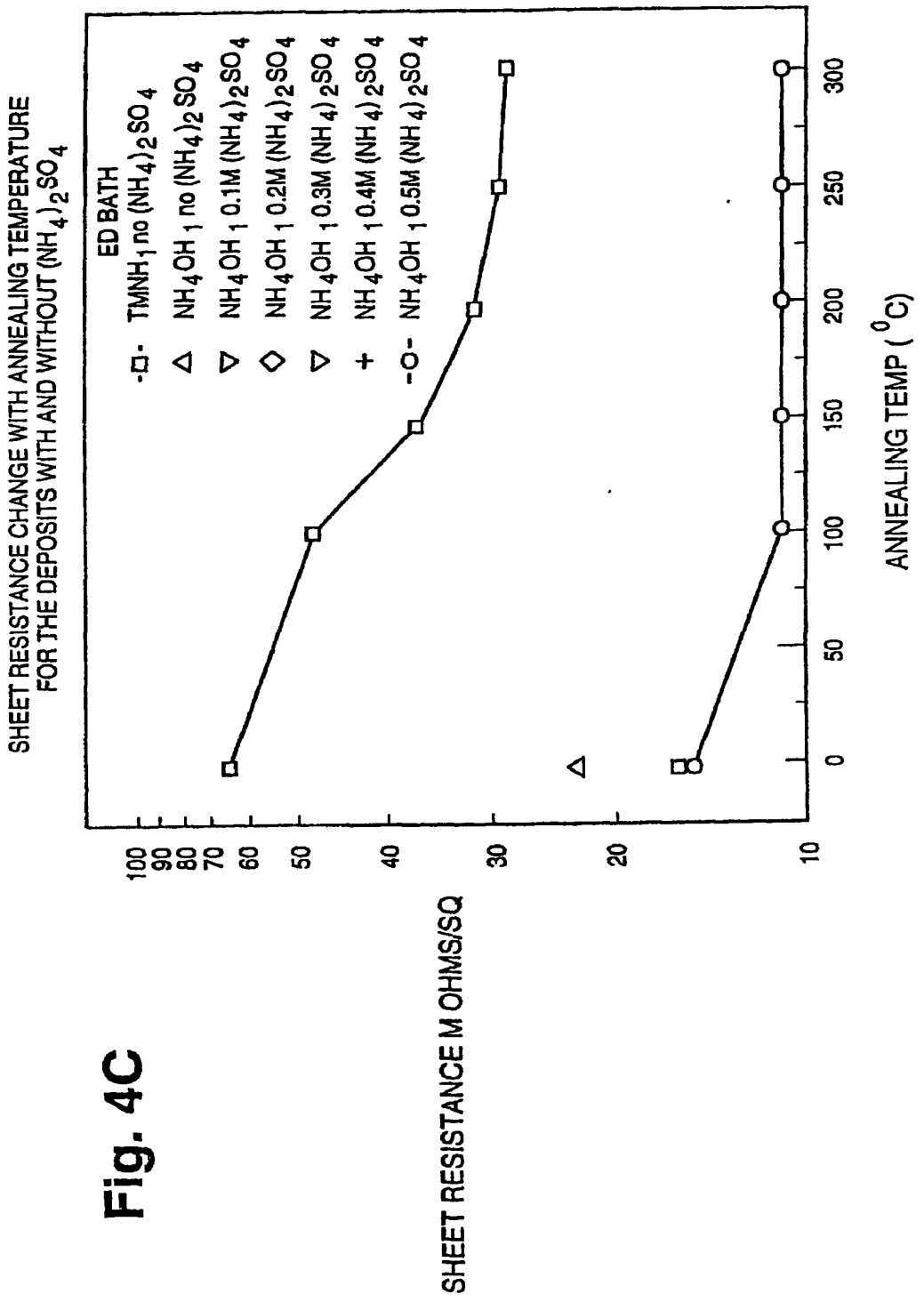

SHEET RESISTANCE CHANGE WITH ANNEALING TEMPERATURE
FOR THE DEPOSITS WITH AND WITHOUT $(NH_4)_2SO_4$
ED BATH
TMNH1 no $(NH_4)_2SO_4$
NH_4OH_1 no $(NH_4)_2SO_4$
NH_4OH_1 0.1M $(NH_4)_2SO_4$
NH_4OH_1 0.2M $(NH_4)_2SO_4$
NH_4OH_1 0.3M $(NH_4)_2SO_4$
NH_4OH_1 0.4M $(NH_4)_2SO_4$
NH_4OH_1 0.5M $(NH_4)_2SO_4$
SHEET RESISTANCE M OHMS/SQ
100
90
80
70
60
50
40
30
20
10
0
50
100
150
200
250
300
ANNEALING TEMP (^{0}C)

Fig. 4C

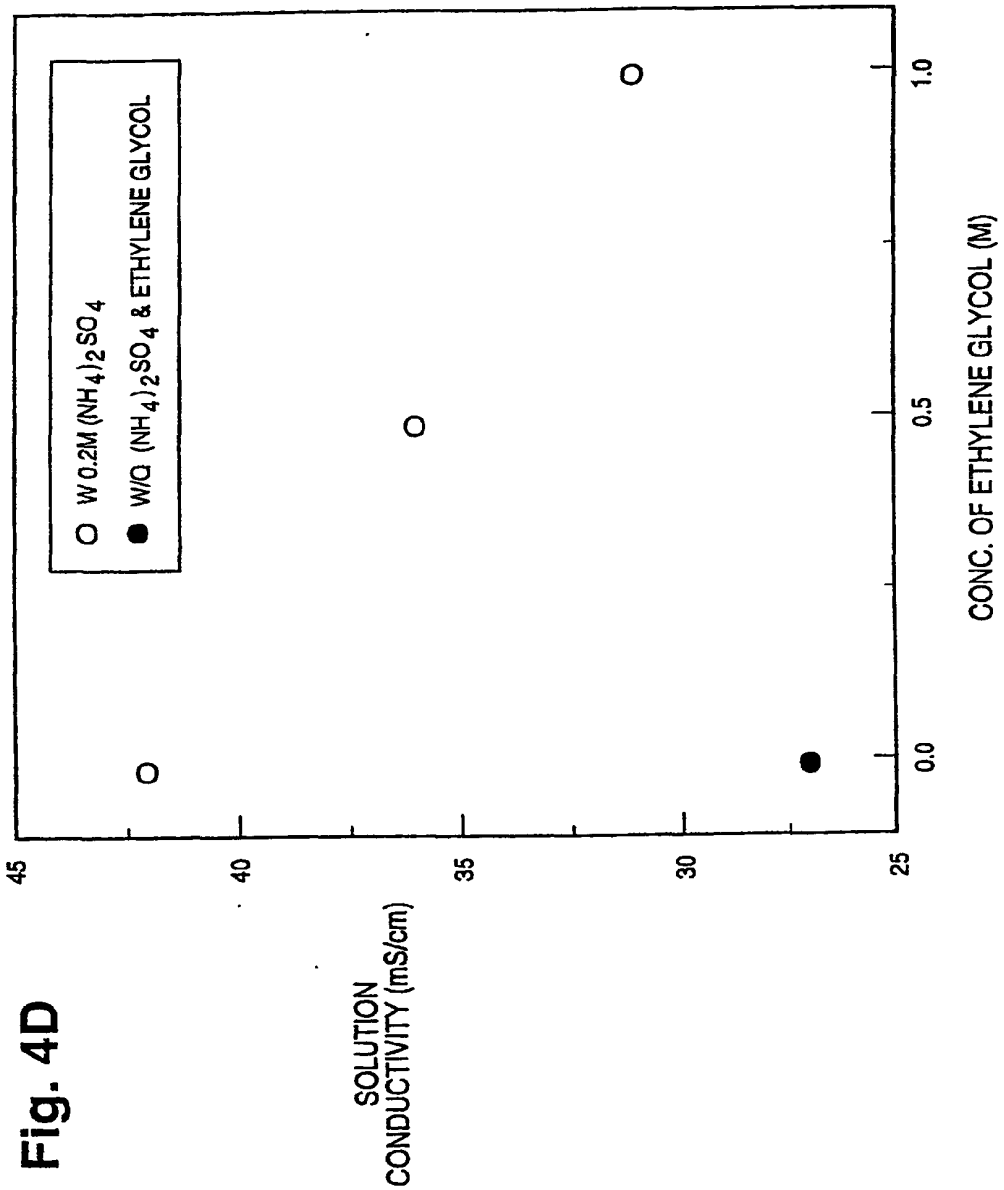

O W/O 0.2M $(NH_4)_2SO_4$
● W/O $(NH_4)_2SO_4$ & ETHYLENE GLYCOL
SOLUTION CONDUCTIVITY (mS/cm)
45
40
35
30
25
0.0
0.5
1.0
CONC. OF ETHYLENE GLYCOL (M)

Fig. 4D

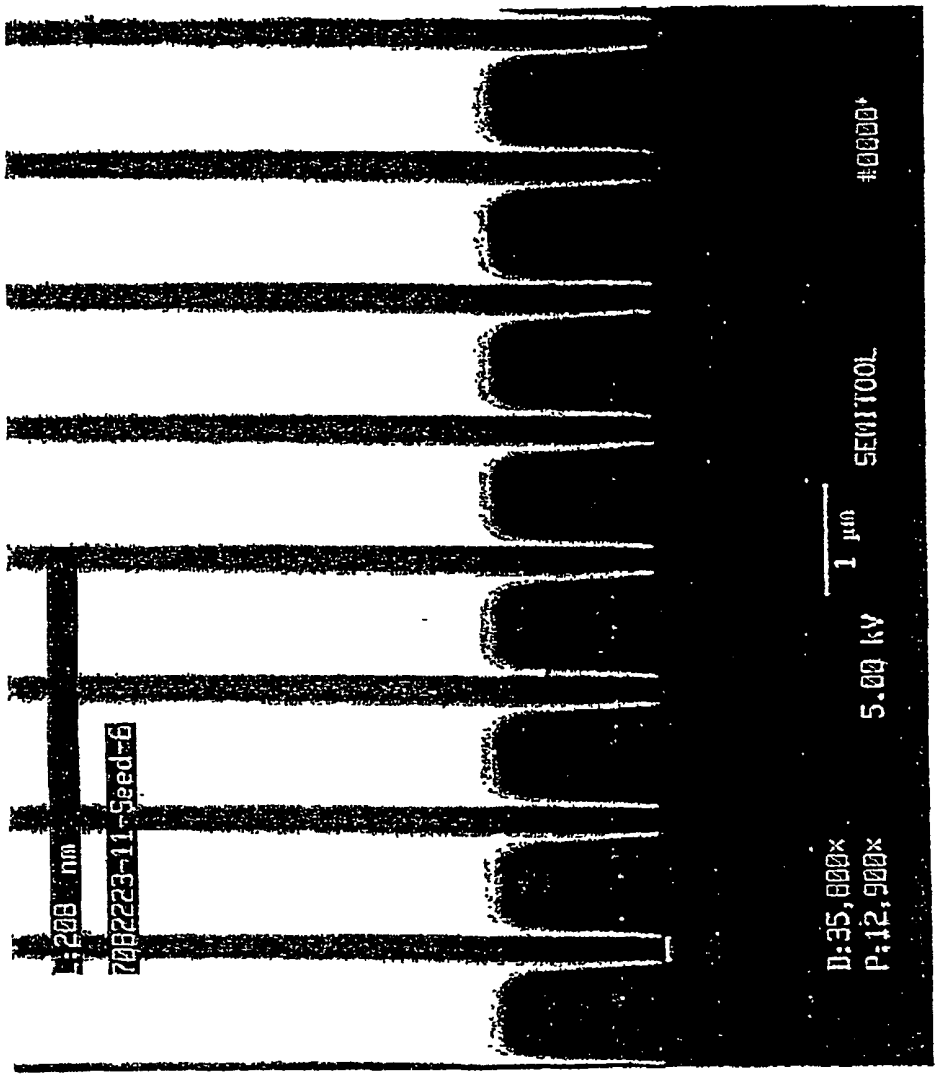

L:208 nm
70B2223-11-Seed-6
D:35,000×
P:12,900×
5.00 kV
1 µm
SEMITOOL
#0000

Fig. 5

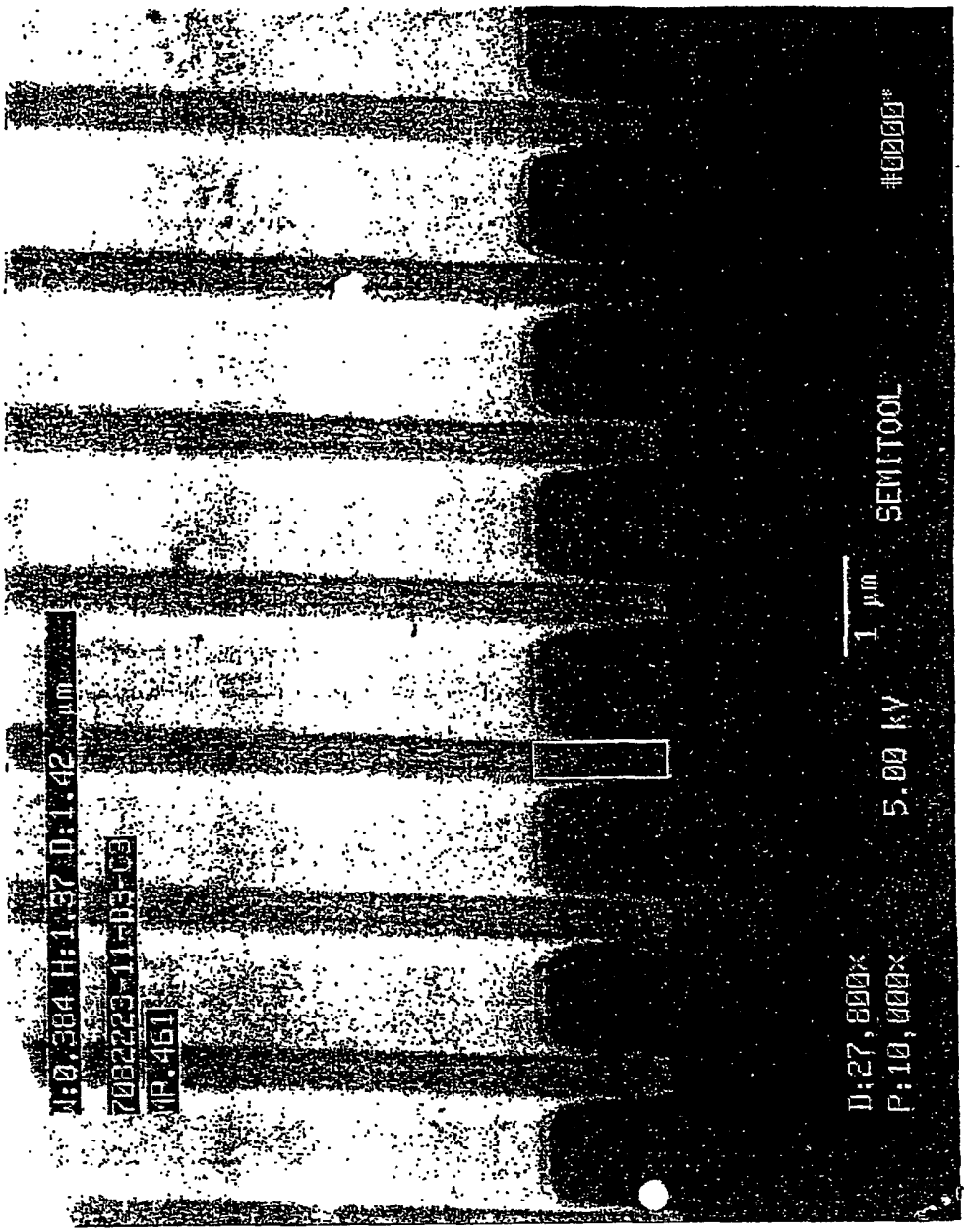

M:0.384 H:1.37 D:1.42 µm
7082229-11-03-03
MP.461
D:27,800x
P:10,000x
5.00 kV
1 µm
SEMITOOL
#0000

Fig. 6A

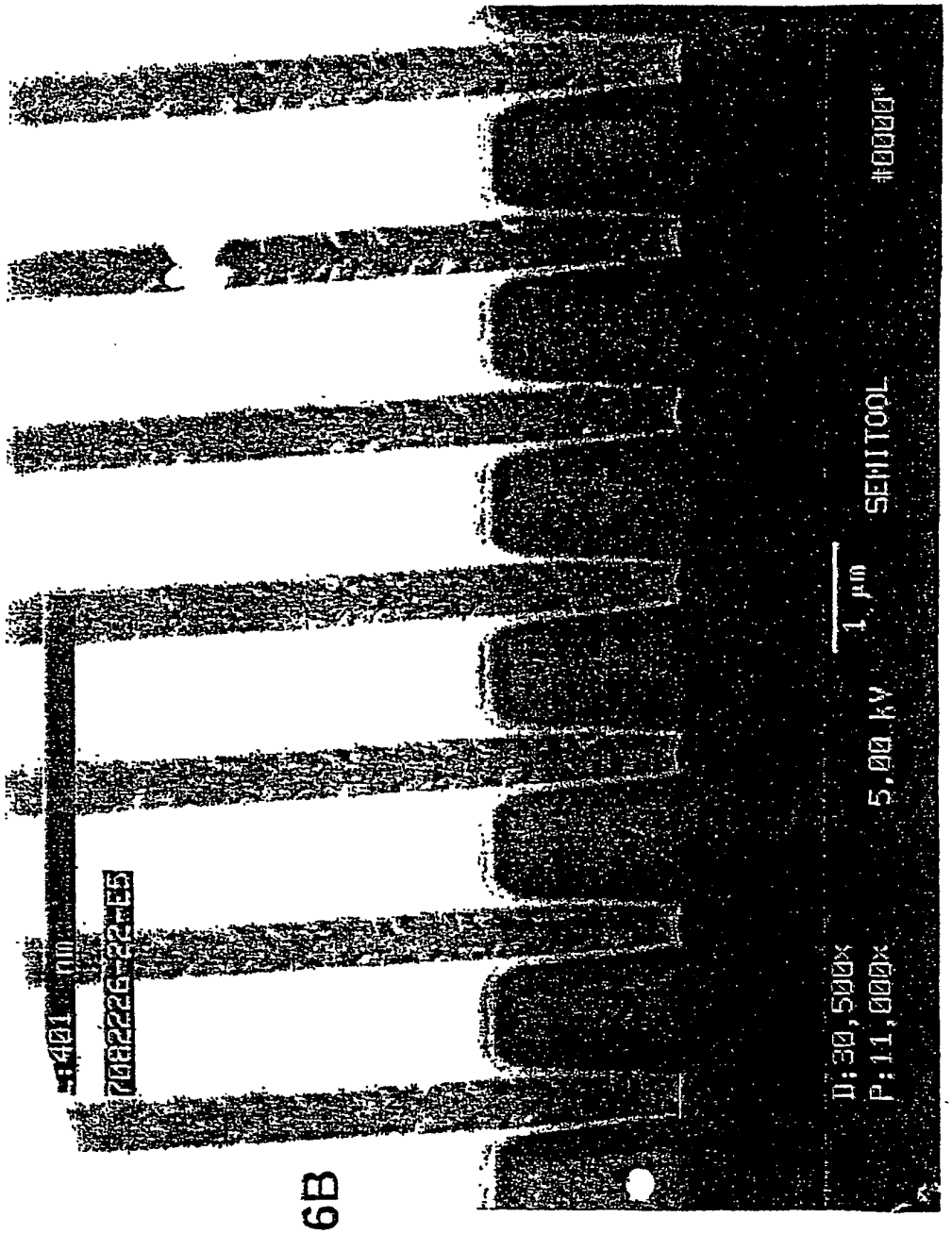
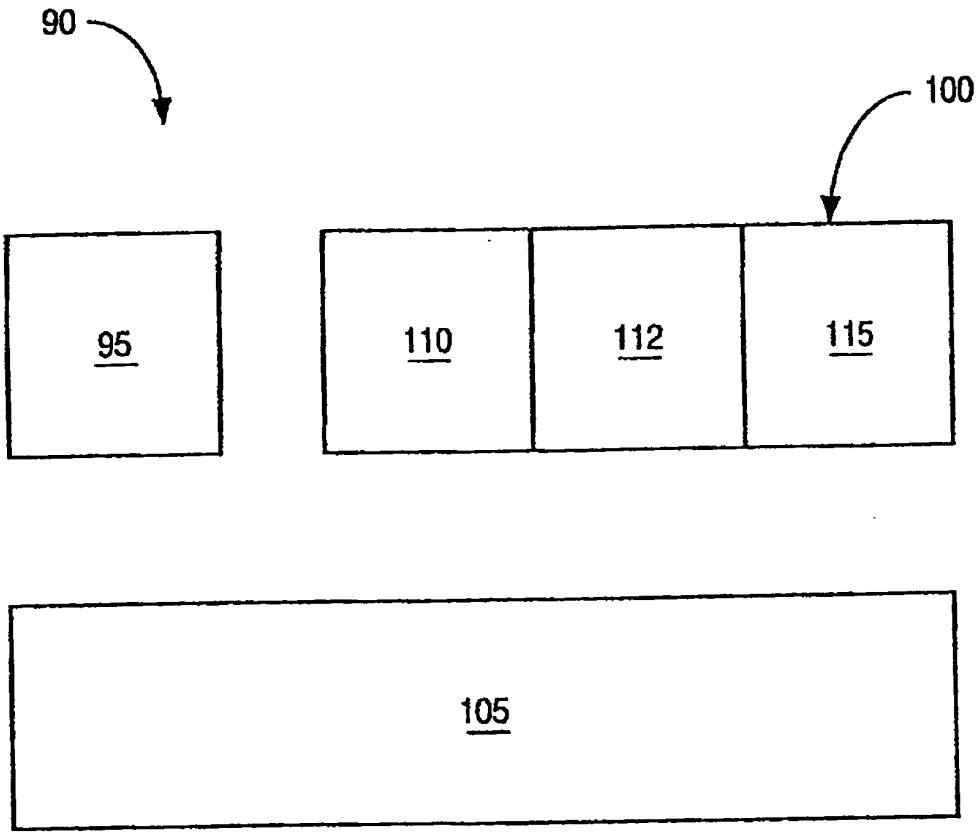


Fig. 6B

Fig. 7



APPARATUS AND METHOD FOR ELECTROLYTICALLY DEPOSITING COPPER ON A SEMICONDUCTOR WORKPIECE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] Not Applicable

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

[0002] Not Applicable

BACKGROUND OF THE INVENTION

[0003] In the fabrication of microelectronic devices, application of one or more metallization layers is often an important step in the overall fabrication process. The metallization may be used in the formation of discrete microelectronic components, such as read/write heads, but it is more often used to interconnect components formed on a workpiece, such as a semiconductor workpiece. For example, such structures are used to interconnect the devices of an integrated circuit.

[0004] A basic understanding of certain terms used herein will assist the reader in understanding the disclosed subject matter. To this end, basic definitions of certain terms, as used in the present disclosure, are set forth below.

[0005] Single Metallization Level is defined as a composite level of a workpiece that is exterior to the substrate. The composite level comprises one or more metal structures.

[0006] Substrate is defined as a base layer of material over which one or more metallization levels are disposed. The substrate may be, for example, a semiconductor wafer, a ceramic block, etc.

[0007] Workpiece is defined as an object that at least comprises a substrate, and may include further layers of material or manufactured components, such as one or more metallization levels, disposed on the substrate.

[0008] An integrated circuit is an interconnected ensemble of devices formed within a semiconductor material and within a dielectric material that overlies a surface of the semiconductor. Devices which may be formed within the semiconductor include MOS transistors, bipolar transistors, diodes and diffused resistors. Devices which may be formed within the dielectric include thin-film resistors and capacitors. Typically, more than 100 integrated circuit die (IC chips) are constructed on a single 8 inch diameter silicon wafer. The devices utilized in each dice are interconnected by conductor paths formed within the dielectric. Typically, two or more levels of conductor paths, with successive levels separated by a dielectric layer, are employed as interconnections. In current practice, an aluminum alloy and silicon oxide are typically used for, respectively, the conductor and dielectric.

[0009] Delays in propagation of electrical signals between devices on a single die limit the performance of integrated circuits. More particularly, these delays limit the speed at which an integrated circuit may process these electrical signals. Larger propagation delays reduce the speed at which the integrated circuit may process the electrical signals, while smaller propagation delays increase this speed. Accordingly, integrated circuit manufacturers seek ways in which to reduce the propagation delays.

[0010] For each interconnect path, signal propagation delay may be characterized by a time delay τ. See E. H. Stevens, *Interconnect Technology*, QMC, Inc., July 1993. An approximate expression for the time delay, τ, as it relates to the transmission of a signal between transistors on an integrated circuit is given below.

$$\tau=RC[1+(V_{SAT}/RI_{SAT})]$$

[0011] In this equation, R and C are, respectively, an equivalent resistance and capacitance for the interconnect path and I_{SAT} and V_{SAT} are, respectively, the saturation (maximum) current and the drain-to-source potential at the onset of current saturation for the transistor that applies a signal to the interconnect path. The path resistance is proportional to the resistivity, ρ, of the conductor material. The path capacitance is proportional to the relative dielectric permittivity, K_e, of the dielectric material. A small value of τ requires that the interconnect line carry a current density sufficiently large to make the ratio V_{SAT}/RI_{SAT} small. It follows therefore, that a low-ρ conductor which can carry a high current density and a low-K_e dielectric must be utilized in the manufacture of high-performance integrated circuits.

[0012] To meet the foregoing criterion, copper interconnect lines within a low-K_e dielectric will likely replace aluminum-alloy lines within a silicon oxide dielectric as the most preferred interconnect structure. See "Copper Goes Mainstream: Low-k to Follow", *Semiconductor International*, November 1997, pp. 67-70. Resistivities of copper films are in the range of 1.7 to 2.0 $\mu\Omega$cm.; resistivities of aluminum-alloy films are in the range of 3.0 to 3.5 $\mu\Omega$cm.

[0013] Despite the advantageous properties of copper, it has not been as widely used as an interconnect material as one would expect. This is due, at least in part, to the difficulty of depositing copper metallization and, further, due to the need for the presence of barrier layer materials. The need for a barrier layer arises from the tendency of copper to diffuse into silicon junctions and alter the electrical characteristics of the semiconductor devices formed in the substrate. Barrier layers made of, for example, titanium nitride, tantalum nitride, etc., must be laid over the silicon junctions and any intervening layers prior to depositing a layer of copper to prevent such diffusion.

[0014] A number of processes for applying copper metallization to semiconductor workpieces have been developed in recent years. One such process is chemical vapor deposition (CVD), in which a thin copper film is formed on the surface of the barrier layer by thermal decomposition and/or reaction of gas phase copper compositions. A CVD process can result in conformal copper coverage over a variety of topological profiles, but such processes are expensive when used to implement an entire metallization layer.

[0015] Another known technique, physical vapor deposition (PVD), can readily deposit copper on the barrier layer with relatively good adhesion when compared to CVD processes. One disadvantage of PVD processes, however, is that they result in poor (non-conformal) step coverage when used to fill microstructures, such as vias and trenches, disposed in the surface of the semiconductor workpiece. For

example, such non-conformal coverage results in less copper deposition at the bottom and especially on the sidewalls of trenches in the semiconductor devices.

[0016] Inadequate deposition of a PVD copper layer into a trench to form an interconnect line in the plane of a metallization layer is illustrated in **FIG. 1**. As illustrated, the upper portion of the trench is effectively "pinched off" before an adequate amount of copper has been deposited within the lower portions of the trench. This result in an open void region that seriously impacts the ability of the metallization line to carry the electrical signals for which it was designed.

[0017] Electrochemical deposition of copper has been found to provide the most cost-effective manner in which to deposit a copper metallization layer. In addition to being economically viable, such deposition techniques provide substantially conformal copper films that are mechanically and electrically suitable for interconnect structures. These techniques, however, are generally only suitable for applying copper to an electrically conductive layer. As such, an underlying conductive seed layer is generally applied to the workpiece before it is subject to an electrochemical deposition process. Techniques for electrodeposition of copper on a barrier layer material have not heretofore been commercially viable.

[0018] The present inventors have recognized that there exists a need to provide copper metallization processing techniques that 1) provide conformal copper coverage with adequate adhesion to the barrier layer, 2) provide adequate deposition speeds, and 3) are commercially viable. These needs are met by the apparatus and processes of the present invention as described below.

BRIEF SUMMARY OF THE INVENTION

[0019] This invention employs a novel approach to the copper metallization of a workpiece, such as a semiconductor workpiece. In accordance with the invention, an alkaline electrolytic copper bath is used to electroplate copper onto a seed layer, electroplate copper directly onto a barrier layer material, or enhance an ultra-thin copper seed layer which has been deposited on the barrier layer using a deposition process such as PVD. The resulting copper layer provides an excellent conformal copper coating that fills trenches, vias, and other microstructures in the workpiece. When used for seed layer enhancement, the resulting copper seed layer provide an excellent conformal copper coating that allows the microstructures to be filled with a copper layer having good uniformity using electrochemical deposition techniques. Further, copper layers that are electroplated in the disclosed manner exhibit low sheet resistance and are readily annealed at low temperatures.

[0020] The disclosed process, as noted above, is applicable to a wide range of steps used in the manufacture of a metallization layer in a workpiece. The workpiece may, for example, be a semiconductor workpiece that is processed to form integrated circuits or other microelectronic components. Without limitation as to the applicability of the disclosed invention, a process for enhancing a seed layer is described.

[0021] A process for applying a metallization interconnect structure to a workpiece having a barrier layer deposited on a surface thereof is also set forth. The process includes the forming of an ultra-thin metal seed layer on the barrier layer. The ultra-thin seed layer has a thickness of less than or equal to about 500 Angstroms and may be formed from any material that can serve as a seed layer for subsequent metal deposition. Such metals include, for example, copper, copper alloys, aluminum, aluminum alloys, nickel, nickel alloys, etc. The ultra-thin seed layer is then enhanced by depositing additional metal thereon in a separate deposition step to provide an enhanced seed layer that is suitable for use in a primary metal deposition. The enhanced seed layer has a thickness at all points on sidewalls of substantially all recessed features distributed within the workpiece that is equal to or greater than about 10% of the nominal seed layer thickness over an exteriorly disposed surface of the workpiece.

[0022] In accordance with a specific embodiment of the process, a copper-containing metallization interconnect structure is formed. To this end, the ultra-thin seed layer is enhanced by subjecting the semiconductor workpiece to an electrochemical copper deposition process in which an alkaline bath having a complexing agent is employed. The copper complexing agent may be at least one complexing agent selected from a group consisting of EDTA, ED, and a polycarboxylic acid such as citric acid or salts thereof.

[0023] Various plating bath compositions suitable for blanket plating, fill-plating of recessed micro-structures, and seed layer enhancement plating are also set forth. A preferred solution for electroplating copper for seed layer enhancement comprises copper sulfate, boric acid, and a complexing agent. The complexing agent is preferably selected from the group consisting of ED, EDTA, and a polycarboxylic acid, such as citric acid. This solution is also suitable for blanket plating and fill-plating of recessed micro-structures.

[0024] A plating solution that improves the resistivity of the resulting copper film is also set forth. The plating solution preferably comprises copper sulfate, ammonium sulfate, and ethylene glycol. This solution is also suitable for blanket plating and fill-plating of recessed micro-structures.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0025] **FIG. 1** is a cross-sectional view illustrating an interconnect line formed completely by PVD copper.

[0026] FIGS. **2A-2E** are cross-sectional views through a semiconductor workpiece illustrating the various layers of material as they are applied in accordance with one embodiment of the present invention.

[0027] **FIG. 3** is a schematic representation of an apparatus suitable for enhancing an ultra-thin seed layer.

[0028] **FIG. 4A** is a graph illustrating the current-potential curves of a plating solution using a polycarboxylic acid, such as citric acid, as a complexing agent.

[0029] **FIG. 4B** a graph illustrating the current-potential curves of a plating solution using EDTA, an amine-containing plating solution, as the complexing agent.

[0030] **FIG. 4C** is a graph of sheet resistance change with annealing temperature for copper films deposited from a bath solution with and without ammonium sulfate.

[0031] **FIG. 4D** is a graph illustrating plating solution conductivity as a function of ethylene glycol concentration in collating solutions with and without ammonium sulfate.

[0032] **FIG. 5** is a scanning eletromicrograph photograph illustrating an ultra-thin seed layer.

[0033] **FIG. 6A** is a scanning eletromicrograph photograph illustrating an ultra-thin seed layer that has been enhanced in a citric acid bath.

[0034] **FIG. 6B** is a scanning eletromicrograph photograph illustrating an ultra-thin seed layer that has been enhanced in an EDTA bath.

[0035] **FIG. 7** is a schematic representation of a section of a semiconductor manufacturing line suitable for implementing the disclosed seed layer enhancement steps.

DETAILED DESCRIPTION OF THE INVENTION

[0036] This invention employs a novel approach to applying copper metallization to a workpiece, such as a semiconductor workpiece. In accordance with the invention, an alkaline electrolytic copper bath is used to electroplate copper onto a seed layer, electroplate copper directly onto a barrier layer material, or enhance an ultra-thin copper seed layer which has been deposited on the barrier layer using a deposition process such as PVD. Additionally, a method for applying a metallization layer will be disclosed. Although the disclosed method may be used in connection with a substantial number of different metal compositions, the specific embodiment disclosed herein is directed to the application of a copper-containing metallization layer. To this end, an alkaline electrolytic copper bath is used to enhance an ultra-thin copper seed layer which has been deposited on a barrier layer using a deposition process such as PVD. The enhanced copper seed layer provides an excellent conformal copper coating that allows trenches and vias to be subsequently filled with a copper layer having good uniformity using electrochemical deposition techniques.

[0037] A cross-sectional view of a micro-structure, such as trench **5**, that is to be filled with copper metallization is illustrated in **FIG. 2A** and will be used to describe the seed layer enhancement aspects of the present invention. As shown, a thin barrier layer **10** of, for example, titanium nitride or tantalum nitride is deposited over the surface of a semiconductor device or, as illustrated in **FIG. 2A**, over a layer of a dielectric **8**, such as silicon dioxide. The barrier layer **10** acts to prevent the migration of copper to any semiconductor device formed in the substrate. Any of the various known techniques, such as CVD or PVD, can be used to deposit the barrier layer depending on the particular barrier material being used. Preferably, the thickness for the barrier layer is approximately 100 to 300 Angstroms.

[0038] After the deposition of the barrier layer, an ultra-thin copper seed layer **15** is deposited on the barrier layer **10**. The resulting structure is illustrated in **FIG. 2B**. Preferably, the copper seed layer **15** is formed using a vapor deposition technique, such as CVD or PVD. In order to have adequate adhesion and copper coverage, a relatively thick (1000 Angstroms) copper seed layer is usually required. Such a thick seed layer leads to problems with close-off of small geometry trenches, however, when a PVD deposition process is employed for applying the seed layer.

[0039] Contrary to traditional thoughts regarding seed layer application, the copper seed layer **15** of the illustrated embodiment is ultra-thin, having a thickness of about 50 to about 500 Angstroms, preferably about 100 to about 250 Angstroms, and most preferably about 200 Angstroms. The ultra-thin copper seed layer can be deposited using a CVD or a PVD process, or a combination of both. PVD is the preferred application process, however, because it can readily deposit copper on the barrier layer **10** with relatively good adhesion. By depositing an ultra-thin seed layer of copper, rather than the relatively thick seed layer used in the prior art, pinching off of the trenches can be avoided.

[0040] The use of an ultra-thin seed layer **15** generally introduces its own set of problems. One of the most significant of these problems is the fact that such ultra-thin layers do not generally coat the barrier layer **10** in a uniform manner. Rather, voids or non-continuous seed layer regions on the sidewalls, such as at **20**, are often present in an ultra-thin seed layer **15** thereby resulting in the inability to properly apply a subsequent electrochemically deposited copper layer in the regions **20**. Further, ultra-thin seed layers tend to include spikes, such as at **21**, that impact the uniformity of the subsequent electrolytically deposited metal layer. Such spikes **21** result in high potential regions at which the copper deposits at a higher rate than at other, more level regions. As such, the seed layer **15** is not fully suitable for the traditional electroplating techniques typically used after application of a seed layer.

[0041] The present inventors have found that an ultra-thin seed layer can be employed if it is combined with a subsequent electrochemical seed layer enhancement technique. To this end, the semiconductor workpiece is subject to a subsequent process step in which a further amount of copper **18** is applied to the ultra-thin seed layer to thereby enhance the seed layer. A seed layer enhanced by the additional deposition of copper is illustrated in **FIG. 2C**. As shown in **FIG. 2C**, the void or non-continuous regions **20** of **FIG. 2B** have been filled thereby leaving substantially all of the barrier layer **10** covered with copper.

[0042] Preferably, the seed layer enhancement process continues until a sidewall step coverage, i.e., the ratio of the seed layer thickness at the bottom sidewall regions **22** to the nominal thickness of the seed layer at the exteriorly disposed side **23** of the workpiece, achieves a value of at least 10%. More preferably, the sidewall step coverage is at least about 20%. Such sidewall step coverage values are present in substantially all of the recessed structures of the semiconductor workpiece. It will be recognized, however, that certain recessed structures distributed within the semiconductor workpiece may not reach these sidewall step coverage values. For example, such structures disposed at the peripheral edges of a semiconductor wafer may not reach these step coverage values. Similarly, defects or contaminants at the situs of certain recessed structures may prevent them from reaching the desired coverage values. The nominal thickness of the enhanced seed layer at the exteriorly disposed side of the workpiece is preferably in the range of 500 angstroms 1600 angstroms.

[0043] Although the embodiment of the process disclosed herein is described in connection with copper metallization,

it is understood that the basic principle of the enhancement of an ultra-thin seed layer prior to the bulk deposition thereof can be applied to other metals or alloys that are capable of being electroplated. Such metals include iron, nickel, cobalt, zinc, copper-zinc, nickel-iron, cobalt-iron, etc.

[0044] A schematic representation of an apparatus **25** suitable for enhancing the ultra-thin copper seed layer is illustrated in **FIG. 3**. It will be recognized that this apparatus is also suitable for applying a blanket plating layer and/or full-fill plating of recessed micro-structures As shown, a semiconductor workpiece, such as a semiconductor wafer **30**, is positioned face down in a bath **35** of electroplating solution. One or more contacts **40** are provided to connect the wafer **30** to a plating power supply **45** as a cathode of an electroplating cell. An anode **50** is disposed in the bath **35** and is connected to the plating power supply **45**. Preferably, a diffuser **55** is disposed between the anode **50** and the wafer/cathode **30**. The wafer **30** may be rotated about axis **60** during the enhancement process. Anode **50** may be provided with a dielectric shield **65** at a backside thereof which faces an incoming stream of plating bath fluid.

[0045] As noted above, certain aspects of the present invention relate to new and useful plating solutions. These solutions can be used for blanket plating, full-fill of the recessed micro-structures, seed layer enhancement, etc. The preferred electrolytic bath solution for enhancing the seed layer is an alkaline copper bath in which copper ions are complexed with a complexing agent. A preferred composition and range of concentrations for the various components of the plating bath include the following:

[0046] 1. Copper sulfate: 0.03M to 0.25M (preferably, 0.04);

[0047] 2. Complexing agent: complex to metal ratios from 1 to 4, preferably 2;

[0048] 3. Boric acid: 0.01M to 0.5M, preferably 0.05M; and

[0049] 4. pH: 5-13, preferably 9.5.

[0050] A preferred source of copper ions is copper sulfate ($CuSO_4$). The concentration of copper sulfate in the bath is preferably within the range of 0.03 to 0.25 M, and is more preferably about 0.1 M.

[0051] Complexing agents that are suitable for use in the present invention form a stable complex with copper ions and prevent the precipitation of copper hydroxide. Ethylene diamine tetracetic acid (EDTA), ethylene diamine (ED), citric acid, and their salts have been found to be particularly suitable copper complexing agents. The molar ratio of complexing agent to copper sulfate in the bath is preferably within the range of 1 to 4, and is preferably about 2. Such complexing agents can be used alone, in combination with one another, or in combination with one or more further complexing agents.

[0052] The electrolytic bath is preferably maintained at a pH of at least 9.0. Potassium hydroxide, ammonium hydroxide, tetramethylammonium hydroxide, or sodium hydroxide is utilized to adjust and maintain the pH at the desired level of 9.0 or above. A preferred pH for a citric acid or ED bath is about 9.5, while a preferred pH for an EDTA bath is about 12.5. As noted above, the complexing agent assists in preventing the copper from precipitating at the high pH level.

[0053] Additional components can be added to the alkaline copper bath. For example, boric acid (H_3BO_3) aids in maintaining the pH at 9.5 when citric acid or ED is used as the complexing agent, and provides brighter copper deposits when added to an electrolytic bath containing EDTA as the complexing agent. If boric acid is added, its concentration in the bath is preferably within the range of 0.01 to 0.5 M.

[0054] In general, the temperature of the bath can be within the range of 20 to 35° C., with 25° C. being a preferred temperature. The current density for electrolytically depositing copper to enhance the copper seed layer can be 1 to 5 milliamps/cm^2, while a plating time of about 1 to about 5 minutes is sufficient to enhance the copper seed layer. The plating waveform may be, for example, a forward periodic pulse having a period of 2 msec at a 50% duty cycle.

[0055] An amine free acid complexing agent, for example, a polycarboxylic acid, such as citric acid, and salts thereof, is preferable to the use of EDTA or ED. EDTA and ED include amine groups. These amine groups often remain on the surface of the semiconductor workpiece after rinsing and drying of the wafer. Subsequent processes, particularly such processes as photolithographic processes, may be corrupted by the reactions resulting from the presence of these amine groups. The amine groups may, for example, interfere with the chemical reactions associated with the exposing and/or curing of photoresist materials. As such, amine free complexing agents are particularly suitable in processes in which a photolithographic process follows an electrodeposition process.

[0056] A further advantage of using a polycarboxylic acid, such as citric acid, stems from the fact that the magnitude of the voltage potential at which the copper is plated is greater than the magnitude of the voltage potential at which the copper is plated in a bath containing EDTA. This is illustrated in **FIGS. 4A and 4B** where **FIG. 4A** is a current-potential graph for a citric acid bath, and **FIG. 4B** is a current-potential graph for an EDTA bath. Electroplating takes place at the voltage where the corresponding current increases abruptly. This plating voltage is referred to as the deposition potential, which is approximately −1.25 volts as shown in **FIG. 4A** for a bath employing citric acid as the complexing agent, and is approximately −1.0 volts as shown in **FIG. 4B** for a bath employing EDTA as the complexing agent. The current peaks (**70**/**70'** for the a bath containing a citric acid, and **72**, **72'** for the bath containing the EDTA) are the limiting currents which are mainly determined by mass transfer and the concentration of copper ions in the plating solutions. As illustrated, the magnitude of the current and the particular plating potential is slightly dependent on the substrate material. The different substrate results are illustrated in **FIGS. 4A and 4B**, where **70** and **72** are the curves for a copper substrate material, and **70'** and **72'** are curves for a copper substrate material comprised of copper with a copper oxide coating. It is noted that additional peaks occur on oxidized copper in the same electrolytes. These peaks are related to the electrochemical reduction of copper oxide to metallic copper before the alkaline electrochemical copper deposition.

[0057] It is believed that a copper layer plated at a higher plating potential in an alkaline bath provides greater adhesion to the underlying barrier layer than a copper layer plated

at a lower plating potential in an acid bath. For copper to adhere to the barrier material, it is thought that copper ions must impinge on the barrier surface with sufficient energy to penetrate a thin oxidized or contaminated layer at the barrier surface. It is therefore believed that a copper layer deposited at a higher magnitude plating potential adhere is better to the exposed barrier layer during the plating process when compared to a layer plated using a smaller magnitude plating potential. This factor, combined with the inter-copper chemical bond between the PVD copper and the electrochemically deposited copper provides for an enhanced seed layer having excellent electrical as well as barrier adhesion properties. Such characteristics are also desirable for films used in blanket plating, full-fill plating, pattern plating, etc.

[0058] It has been found that the resistivity of the deposited copper film is directly related to the resistivity of the plating bath solution. Additives that assist in lowering the resistivity of the solution therefore provide a corresponding reduction in the resistivity of the deposited film.

[0059] Experimental results indicate that addition of ammonium sulfate significantly reduces the resistivity of the plating bath solution and, as such, the deposited film. The sheet resistance obtained for different amounts of ammonium sulfate are compared in the graph **FIG. 4C**. As can be seen, the highest sheet resistance, either with or without annealing at high temperatures, was obtained in the bath containing no ammonium sulfate. If ammonium hydroxide was used to adjust pH in which a trace amount of ammonium sulfate is introduced to the bath, the sheet resistance was reduced from 76 to 23. As the concentration of ammonium sulfate increased from 0.1 M to 0.5 M, the sheet resistance continuously decreased in a corresponding manner.

[0060] Although ammonium sulfate assists in reducing the sheet resistance of the deposited copper layer, experimental results indicate that it reduces the conformality of the resulting copper film. However, the addition of ethylene glycol to the ammonium sulfate containing solution substantially increases the conformality of the resulting deposit. **FIG. 4D** illustrates the relationship between the concentration of ethylene glycol and the conductivity of a plating solution containing 0.2M the of ammonium sulfate.

[0061] A preferred composition and range of concentrations for the various components of a plating bath having ammonium sulfate include the following:

[0062] 1. Copper sulfate: 0.03M to 0.5M (preferably, 0.25M);

[0063] 2. Complexing agent: complex to metal ratios from 1 to 4, preferably 2 using ED;

[0064] 3. Ammonium sulfate: 0.01M to 0.5M, preferably 0.3M; and

[0065] 4. Boric acid: 0.00 to 0.5M, preferably 0.2M.

[0066] As noted above, such a bath composition can be used for blanket plating, pattern plating, full-fill plating, and seed layer enhancement.

[0067] With reference again to the specific seed layer enhanced aspects of the present invention, the enhanced seed layer of **FIG. 2C** is suitable for subsequent electrochemical copper deposition. This subsequent copper deposition may take place in an alkaline bath within the apparatus employed to enhance the seed layer. This may be followed by a low-temperature annealing process that assists in lowering the resistivity of the deposited copper. Such a low-temperature annealing process preferably takes place at a temperature below about the 250 degrees Celsius and, more preferably, below about 100 degrees Celsius. When a low-K dielectric material is employed to isolate the copper structures, the upper annealing temperature limit should be chosen to be below the degradation temperature of the dielectric material.

[0068] Although the foregoing alkaline bath compositions may be used for the entire electrochemical deposition process, subsequent copper deposition may take place in an acid environment where plating rates are substantially higher than corresponding rates associated with alkaline plating baths. To this end, the semiconductor workpiece is preferably transferred to an apparatus wherein the workpiece is thoroughly rinsed with deionized water and then transferred to an apparatus similar to that of **FIG. 3** wherein the plating bath is acidic. For example, one suitable copper bath comprises 170 g/l H_2SO_4, 17 g/l copper and 70 ppm Chloride ions with organic additives. The organic additives are not absolutely necessary to the plating reaction. Rather, the organic additives may be used to produce desired film characteristics and provide better filling of the recessed structures on the wafer surface. The organic additives may include levelers, brighteners, wetting agents and ductility enhancers. It is during this deposition process that the trench **5** is substantially filled with a further layer of electrochemically deposited copper **22**. The resulting filled cross-section is illustrated in **FIG. 2D**. After being filled in this manner, the barrier layer and the copper layers disposed above the trench are removed using any suitable process thereby leaving only the trench **5** with the copper metallization and associated barrier material as shown in **FIG. 2E**.

[0069] Use of an alkaline electrolytic bath to enhance the copper seed layer has particular advantages over utilizing acid copper baths without seed layer enhancement. After deposition of the PVD copper seed layer, the copper seed layer is typically exposed to an oxygen-containing environment. Oxygen readily converts metallic copper to copper oxide. If an acid copper bath is used to plate copper onto the seed layer after exposure of the seed layer to an oxygen containing environment, the acid copper bath would dissolve copper oxide that had formed, resulting in voids in the seed layer and poor uniformity of the copper layer deposited on the seed layer. Use of an alkaline copper bath in accordance with the disclosed embodiment avoids the problem by advantageously reducing any copper oxide at the surface of the seed layer to metallic copper. Another advantage of the alkaline copper bath is that the plated copper has much better adhesion to the barrier layer than that plated from an acid copper bath. Additional advantages of the seed layer enhancement aspects of the present invention can be seen from the following Example.

EXAMPLE 1

[0070] Comparison of Acid Copper Plating with and without Seed Layer Enhancement

[0071] Semiconductor wafers 1, 2 and 3 were each coated with a 200 Angstrom PVD copper seed layer. In accordance with the present invention, wafers 1 and 2 had seed layer

enhancement from citric acid and EDTA baths, respectively, the compositions of which are set forth below:

[0072] Bath for Wafer 1: 0.1 M Cu SO_4+0.2 M Citric acid+0.05 M H_3BO_3 in D.I. water at pH 9.5, temperature 25° C.

[0073] Bath for Wafer 2: 0.1 M Cu SO_4+0.2 M EDTA acid+0.05 H_3BO_3 in D.I. water at pH 12.5, temperature 25° C.

[0074] Wafer 3 did not have any seed layer enhancement.

[0075] The three wafers were then plated with a 1.5 micron copper layer from an acid copper bath under identical conditions. The following Table compares the uniformities, as deduced from sheet resistance measurements, of the three wafers after the deposition of a copper layer having a nominal thickness of 1.5 microns.

TABLE 1

Wafer	Enhancement Bath	Current Density	Non-uniformity Standard deviation (%, 1σ)
1	Citrate	3 min. at 2 mA/cm^2	7.321
2	EDTA	3 min. at 2 mA/cm^2	6.233
3	None	0	46.10

[0076] As can be seen from the results in Table 1 above, seed layer enhancement in accordance with the disclosed process provides excellent uniformity (6 to 7%) compared to that without seed layer enhancement (46%). This is consistent with observations during visual examination of the wafer after 1.5 micron electroplated copper had been deposited. Such visual examination of the wafer revealed the presence of defects at wafer electrode contact points on the wafer without seed layer enhancement.

[0077] **FIGS. 5, 6A** and **6B** are photographs taken using a SEM. In **FIG. 5**, an ultra-thin seed layer has been deposited on the surface of a semiconductor wafer, including microstructures, such as trenches **85**. As shown, void regions are present at the lower corners of the trenches. In **FIG. 6A**, the seed layer has been enhanced in the manner described above in a bath containing citric acid as the complexing agent. This enhancement resulted in a conformal copper seed layer that is very suited for subsequent electrochemical deposition of copper metallization.

[0078] **FIG. 6B** illustrates a seed layer that has been enhanced in a bath containing EDTA as the complexing agent. The resulting seed layer includes larger grain sizes that project as spikes from the sidewalls of the trenches. These sidewall grain projections make subsequent electrochemical deposition filling of the trenches more difficult since they localize a higher plating rate resulting in non-uniformity of the subsequent electrochemical deposition. This effect is particularly noticeable in recessed microstructures having small dimensions. As such, a complexing agent such as citric acid is more preferable when filling small micro-structures. Results comparable for copper baths containing citric acid have also been achieved using ED as the complexing agent.

[0079] **FIG. 7** is a schematic representation of a section of a semiconductor manufacturing line **90** suitable for implementing the foregoing processes. The line **90** includes a vapor deposition tool or tool set **95** and an electrochemical copper deposition tool or tool set **100**. Transfer of wafers between the tools/tool sets **95** and **100** may be implemented manually or through an automated transfer mechanism **105**. Preferably, automated transfer mechanism **105** transfers workpieces in a pod or similar environment. Alternatively, the transfer mechanism **105** may transfer wafers individually or in an open carrier through a clean atmosphere joining the tools/tool sets.

[0080] In operation, vapor deposition tool/tool set **95** is utilized to apply an ultra-thin copper seed layer over at least portions of semiconductor workpieces that are processed on line **90**. Preferably, this is done using a PVD application process. Workpieces with the ultra-thin seed layer are then transferred to tool/tool set **100**, either individually or in batches, where they are subject to electrochemical seed layer enhancement at, for example, processing station **110**. Processing station **110** may be constructed in the manner set forth in **FIG. 3**. After enhancement is completed, the workpieces are subject to a full electrochemical deposition process in which copper metallization is applied to the workpiece to a desired interconnect metallization thickness. This latter process may take place at station **110**, but preferably occurs at further processing station **115** which deposits the copper metallization in the presence of an acidic plating bath. Before transfer to station **115**, the workpiece is preferably rinsed in DI water at station **112**. Transfer of the wafers between stations **110, 112**, and **115** may be automated by a wafer conveying system **120**. The electrochemical deposition tool set **100** may be implemented using, for example, an LT-210™ model or an Equinox™ model plating tool available from Semitool, Inc., of Kalispell, Mont.

[0081] Numerous modifications may be made to the foregoing system without departing from the basic teachings thereof. Although the present invention has been described in substantial detail with reference to one or more specific embodiments, those of skill in the art will recognize that changes may be made thereto without departing from the scope and spirit of the invention as set forth in the appended claims.

1. A process for applying a metal structure to a workpiece comprising the step of electroplating a copper layer onto a surface of the workpiece using an electroplating bath comprising copper sulfate, ammonium sulfate, a completing agent, and ethylene glycol.

2. A process as set forth in claim 1 wherein the electroplating bath further comprises boric acid.

3. A process as set forth in claim 2 wherein the complexing agent is selected from the group consisting of ED, EDTA, and a polycarboxylic acid.

4. A process for applying a metal structure to a workpiece comprising the step of electroplating a copper layer onto a surface of the workpiece using an electroplating bath comprising copper sulfate, boric acid, and a complexing agent.

5. A process as set forth in claim 4 wherein the complexing agent is selected from the group consisting of ED, EDTA, and a polycarboxylic acid.

6. A process as set forth in claim 4 wherein the complexing agent is citric acid.

7. A process for applying a metallization interconnect structure to a workpiece, the workpiece including a barrier layer deposited on a surface thereof, the process comprising the steps of:

(a) forming an ultra-thin metal seed layer on the barrier layer, the seed layer having a thickness of less than or equal to about 500 Angstroms;

(b) enhancing the ultra-thin seed layer by depositing additional metal to provide an enhanced seed layer, the enhanced seed layer having a thickness at all points on sidewalls of substantially all recessed features distributed within the workpiece that is equal to or greater than about 10% of the nominal seed layer thickness over an exteriorly disposed surface of the workpiece.

8. The process of claim 7 wherein the additional metal is copper.

9. The process of claim 7 wherein the ultra-thin seed layer is enhanced by a process comprising an electrochemical deposition step.

10. The process of claim 9 wherein the electrochemical deposition step occurs in an alkaline bath.

11. The process of claim 10 wherein the alkaline bath comprises metal ions and an agent effective in complexing the metal ions.

12. The process of claim 7 wherein the ultra-thin metal seed layer formed in step (a) is formed by physical vapor deposition.

13. The process of claim 7 wherein the ultra-thin metal seed layer formed in step (a) has a thickness of about 50 to about 500 Angstroms.

14. The process of claim 13 wherein the ultra-thin metal layer formed in step (a) has a thickness of about 100 to about 250 Angstroms.

15. The process of claim 7 wherein the complexing agent is comprised of one or more complexing agents selected from EDTA, ED, and polycarboxylic acid.

16. The process of claim 17 wherein the completing agent is comprised of EDTA and the EDTA in the bath has a concentration within the range of 0.03 to 1.0 M.

17. The process of claim 15 wherein the complexing agent is comprised of ED and wherein the ED in the electrolytic bath has a concentration within the range of 0.03 to 1.0 M.

18. The process of claim 16 wherein the complexing agent is comprised of EDTA and the EDTA has a concentration within the range of 0.1 to 0.4 M.

19. The process of claim 15 wherein the complexing agent is comprised of citric acid and the citric acid in the bath has a concentration within the range of 0.03 to 1.0 M.

20. The process of claim 10 and further comprising the step of subjecting the workpiece to a further electrochemical deposition process in an acidic electrolytic solution to complete deposition of the metal to a thickness needed for the formation of the interconnect structure.

21. The process of claim 20 and further comprising the step of subjecting the workpiece to a rinsing process after electrochemical deposition in the outline bath and prior to the further electrochemical copper deposition process in an acidic electrolytic solution.

22. In a manufacturing line including a plurality of apparatus for the manufacture of integrated circuits, one or more apparatus of the plurality of apparatus being used for applying a copper metallization interconnect structure to a surface of a workpiece used to form the integrated circuits, the one or more apparatus comprising:

means for applying a conductive ultra-thin seed layer to a surface of the workpiece;

means for electrochemically enhancing the conductive ultra-thin seed layer to render it suitable for subsequent electrochemical application of the copper interconnect metallization to a predetermined thickness representing a bulk portion of the copper interconnect metallization structure.

23. One or more apparatus as claimed in claim 22 wherein the means for applying is further defined by means for applying a conductive ultra-thin copper seed layer to a barrier layer surface of the workpiece.

24. One or more apparatus as claimed in claim 22 wherein the means for applying is further defined by means for applying a conductive ultra-thin copper seed layer to a barrier layer surface of the workpiece using a PVD process.

25. One or more apparatus as claimed in claim 22 wherein the means for applying is further defined by means for applying a conductive ultra-thin copper seed layer to a barrier layer surface of the workpiece using a CVD process.

26. One or more apparatus as claimed in claim 23 wherein the means for electrochemically enhancing the conductive ultra-thin seed layer is further defined by means for electrochemically enhancing the conductive ultra-thin seed layer by electrochemically depositing copper using an alkaline copper bath having a complexing agent.

27. One or more apparatus as claimed in claim 26 wherein the electrochemical enhancement of the ultra-thin seed layer takes place at a plating voltage having a magnitude that is at least about or greater than 1.1 volts.

28. One or more apparatus as claimed in claim 26 wherein the alkaline bath has a pH > or equal to about 9.0.

29. One or more apparatus as claimed in claim 26 wherein the complexing agent is comprised of EDTA.

30. One or more apparatus as claimed in claim 26 wherein the complexing agent is comprised of ED.

31. One or more apparatus as claimed in claim 26 wherein the complexing agent is a comprised of a carboxylic acid or salt thereof.

32. One or more apparatus as claimed in claim 31 wherein the complexing agent is citric acid or salt thereof.

33. One or more apparatus as claimed in claim 26 and further comprising means for electrochemically adding a further layer of copper over the conductive ultra-thin seed layer by electrochemically depositing copper using an acidic copper bath.

34. One or more apparatus as claimed in claim 33 wherein the electrochemical enhancement of the ultra-thin seed layer takes place at a plating voltage having a magnitude that is greater than the magnitude of the plating voltage in the acidic copper bath.

35. One or more apparatus as claimed in claim 34 and further comprising means for rinsing the workpiece prior to its introduction to the means for electrochemically adding a further layer of copper.

36. A process for applying a metallization interconnect structure to a workpiece, the workpiece including a barrier layer deposited on a surface thereof, the process comprising the steps of:

(a) forming an ultra-thin metal seed layer on the barrier layer, the seed layer having a thickness of less than or equal to about 500 Angstroms;

(b) subjecting the workpiece to an electrochemical copper deposition process in an alkaline electrolytic bath having copper ions complexed with a complexing agent such that additional copper is deposited on the ultra-thin copper seed layer to thereby enhance the seed layer.

37. The process of claim 36 wherein the ultra-thin metal seed layer formed in step (a) is formed by physical vapor deposition.

38. The process of claim 36 wherein the ultra-thin seed layer formed in step (a) has a thickness of about 50 to about 500 Angstroms.

39. The process of claim 38 wherein the ultra-thin seed layer formed in step (a) has a thickness of about 100 to about 250 Angstroms.

40. The process of claim 39 wherein the ultra-thin seed layer formed in step (a) has a thickness of about 200 Angstroms.

41. The process of claim 36 wherein the alkaline electrolytic bath has a pH of at least 9.0.

42. The process of claim 36 wherein the copper ions in the electrolytic bath are provided by copper sulfate.

43. The process of claim 42 wherein the copper sulfate in the electrolytic bath has a concentration within the range of 0.03 to 0.25 M.

44. The process of claim 42 wherein the concentration of copper sulfate is about 0.1 M.

45. The process of claim 36 wherein the copper complexing agent is comprised of a copper complexing agent selected from EDTA, ED, and citric acid.

46. The process of claim 45 wherein the complexing agent is comprised of EDTA and the EDTA in the electrolytic bath has a concentration within the range of 0.03 to 1.0 M.

47. The process of claim 45 wherein the complexing agent is comprised of ED and the ED in the electrolytic bath has a concentration within the range of 0.03 to 1.0 M.

48. The process of claim 45 wherein the complexing agent is comprised of EDTA and the EDTA has a concentration within the range of 0.1 to 0.4 M.

49. The process of claim 45 wherein the complexing agent is comprised of citric acid and the citric acid in the electrolytic bath has a concentration within the range of 0.03 to 1.0 M.

50. The process of claim 49 wherein the citric acid has a concentration within the range of 0.1 to 0.4 M.

51. The process of claim 36 and further comprising the step of subjecting the workpiece to a further electrochemical copper deposition process in an acidic electrolytic solution to complete deposition of the copper to a thickness needed for the formation of the copper interconnect structure.

52. The process of claim 51 and further comprising the step of subjecting the workpiece to a rinsing process after step (b) and prior to the further electrochemical copper deposition process in an acidic electrolytic solution.

53. A workpiece comprising:

a plurality of the recessed structures distributed in a face of the workpiece;

an enhanced seed layer having a thickness at all points on sidewalls of substantially all recessed features distributed within the workpiece that is equal to or greater than about 10% of the nominal seed layer thickness over an exteriorly disposed surface of the workpiece.

54. A workpiece as claimed in claim 54 wherein the thickness of the sidewalls of substantially all recessed features is equal to or greater than about 20%.

55. A solution for electroplating copper, the solution comprising copper sulfate, ammonium sulfate, and ethylene glycol.

56. The solution of claim 55 and further comprising a complexing agent.

57. A solution for electroplating copper, the solution comprising copper sulfate, boric acid, and a complexing agent.

58. The solution of claim 57 wherein the complexing agent is selected from the group consisting of ED, EDTA, and a polycarboxylic acid.

59. The solution of claim 57 wherein the complexing agent is citric acid.

* * * * *

US006528412B1

(12) **United States Patent**
Wang et al.

(10) **Patent No.: US 6,528,412 B1**
(45) **Date of Patent: Mar. 4, 2003**

(54) **DEPOSITING AN ADHESION SKIN LAYER AND A CONFORMAL SEED LAYER TO FILL AN INTERCONNECT OPENING**

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(73) Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/844,727**

(22) Filed: **Apr. 30, 2001**

(51) **Int. Cl.**[7] **H01L 21/4763**

(52) **U.S. Cl.** **438/628**; 438/622; 438/624; 438/627; 438/637; 438/644; 438/687

(58) **Field of Search** 438/618, 622, 438/624, 626, 627, 628, 633, 637, 642, 643, 644, 652, 653, 654, 675, 680, 681, 648, 687; 257/751, 762

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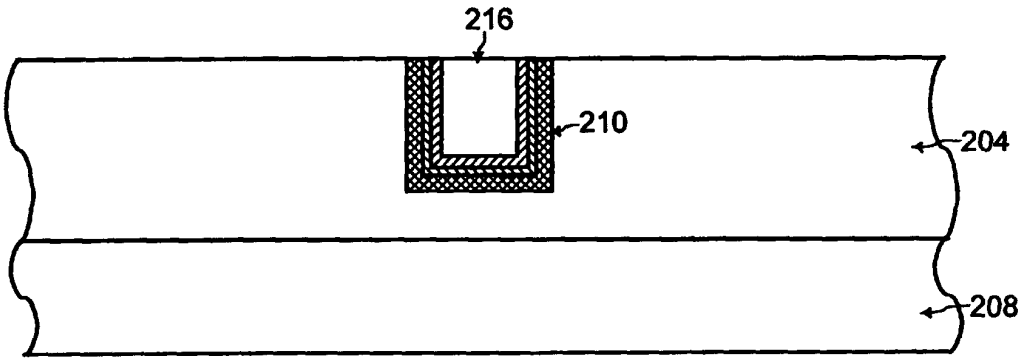
Primary Examiner—Amir Zarabian
Assistant Examiner—Maria Guerrero
(74) *Attorney, Agent, or Firm*—Monica H. Choi

(57) **ABSTRACT**

For filling an interconnect opening within an insulating layer on a semiconductor wafer, an adhesion skin layer is deposited conformally onto an underlying material comprised of one of a barrier material or a dielectric material at sidewalls and a bottom wall of the interconnect opening. The adhesion skin layer includes a metal alloy doping element. A conformal seed layer is deposited onto the adhesion skin layer using a conformal deposition process, such as an ECD (electrochemical deposition) or a CVD (chemical-vapor-deposition) process. The adhesion skin layer promotes adhesion of the conformal seed layer to the underlying material at the sidewalls and the bottom wall of the interconnect opening. The interconnect opening is filled with a conductive material grown from the conformal seed layer. In this manner, the adhesion skin layer promotes adhesion of the conformal seed layer to the underlying material to minimize electromigration failure of the interconnect. In addition, the seed layer formed by conventional PVD (physical-vapor-deposition) processes is avoided with the present invention. Instead, the relatively thin adhesion skin layer and the relatively thin conformal seed layer are used for plating the conductive fill. With such relatively thin layers, an interconnect opening having a high aspect ratio is filled with minimized void formation.

17 Claims, 8 Drawing Sheets



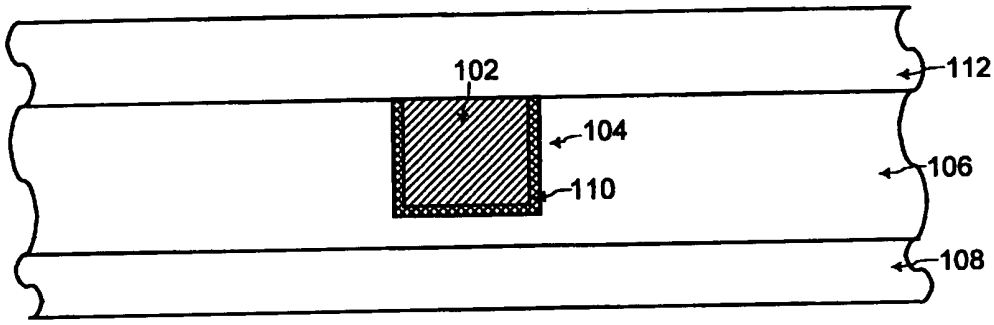


FIG. 1 (Prior Art)

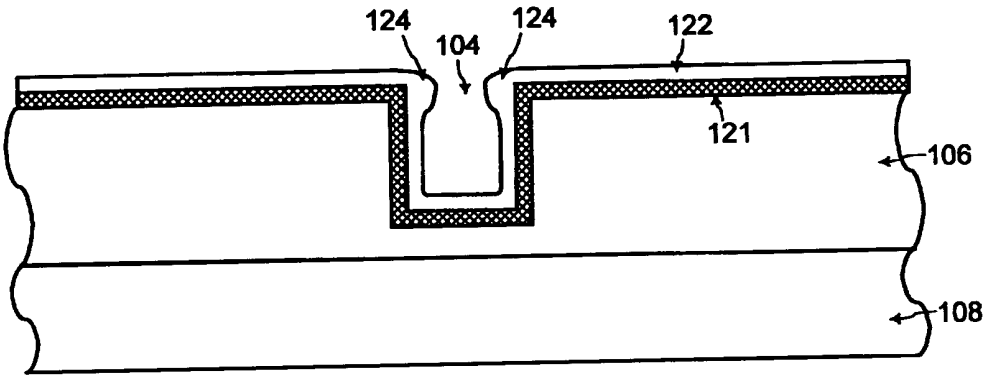


FIG. 2 (Prior Art)

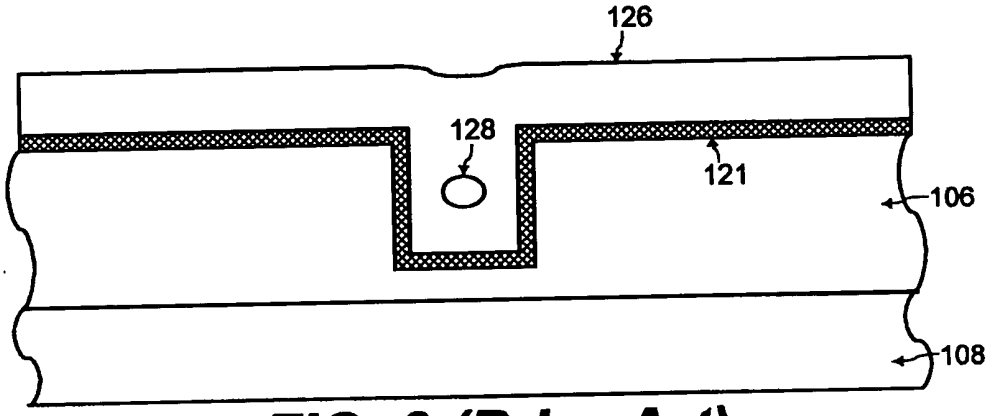


FIG. 3 (Prior Art)

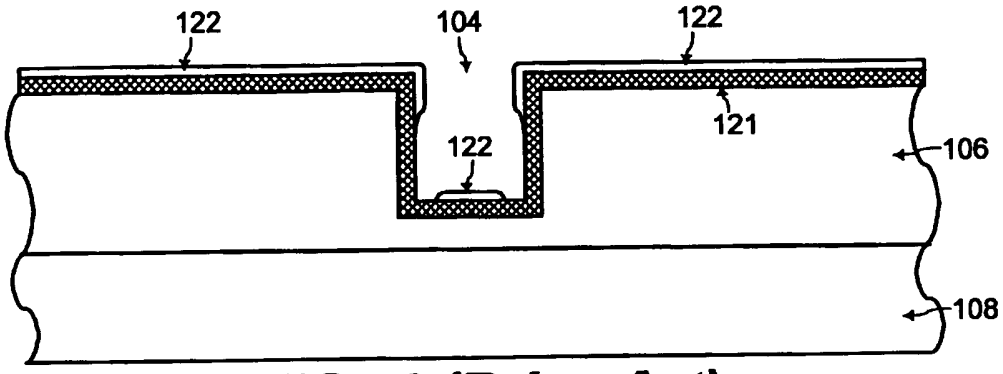


FIG. 4 (Prior Art)

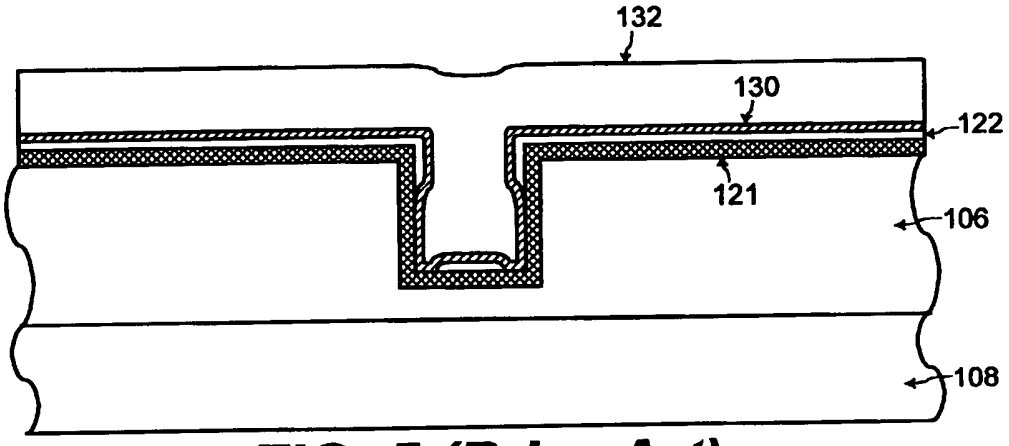


FIG. 5 (Prior Art)

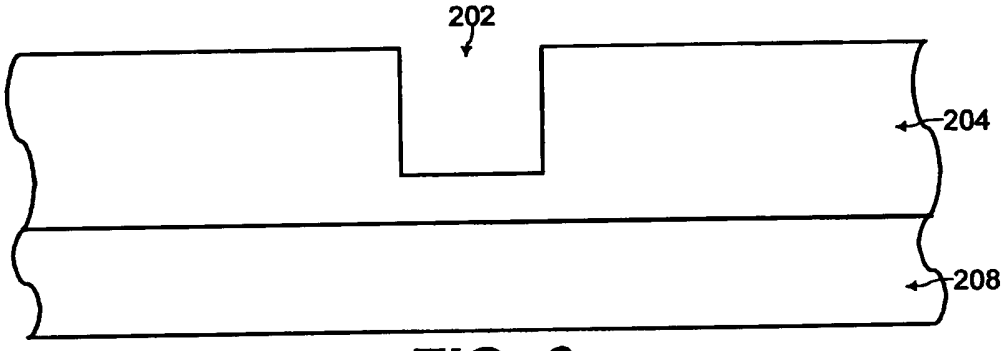


FIG. 6

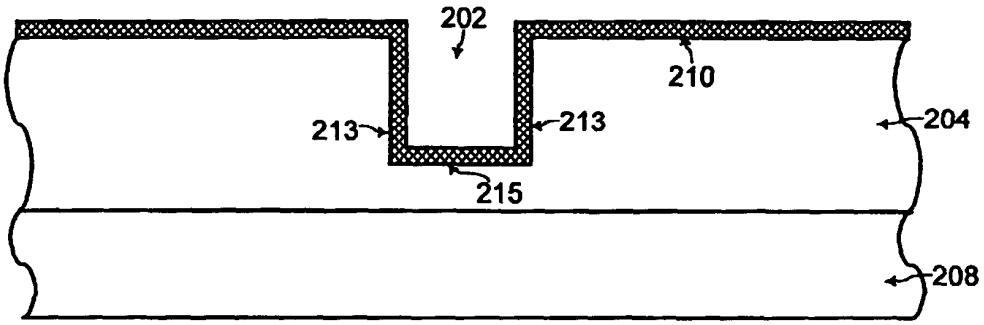


FIG. 7

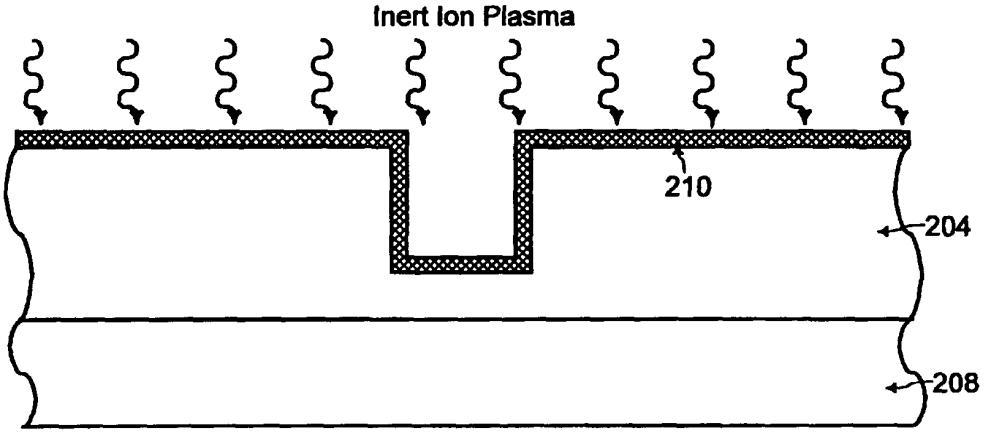


FIG. 8

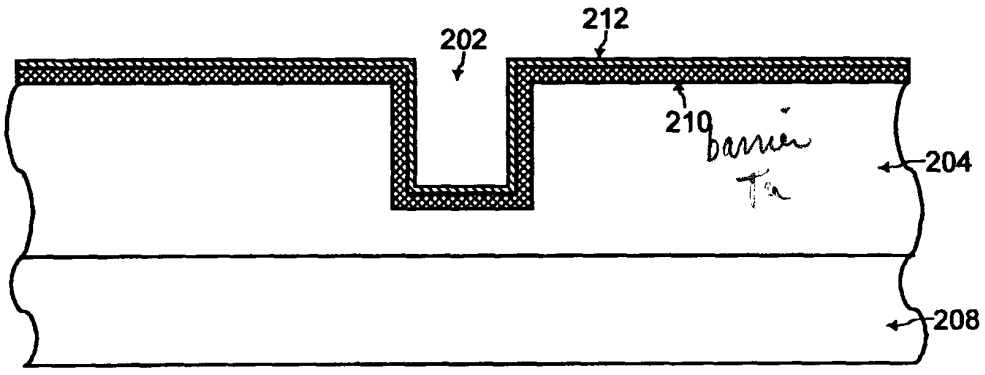


FIG. 9

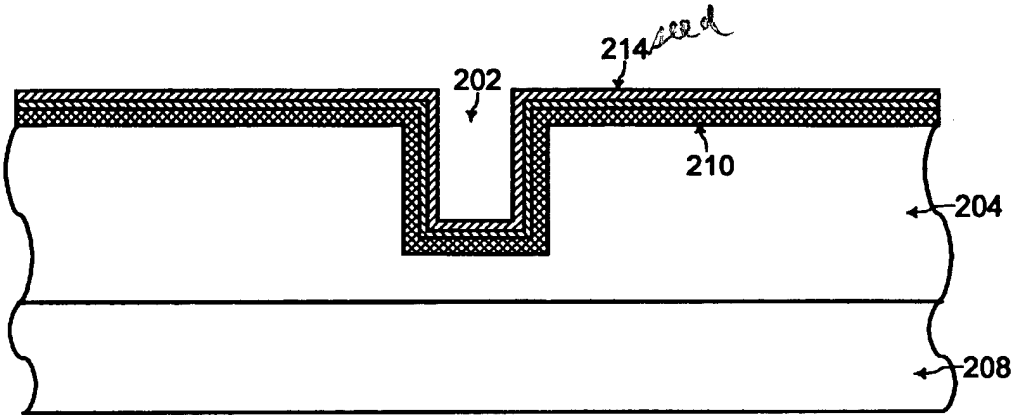


FIG. 10

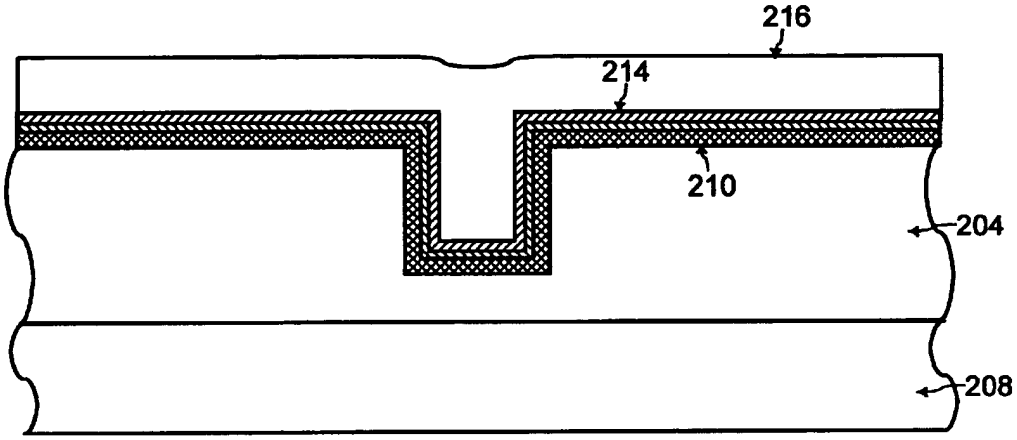


FIG. 11

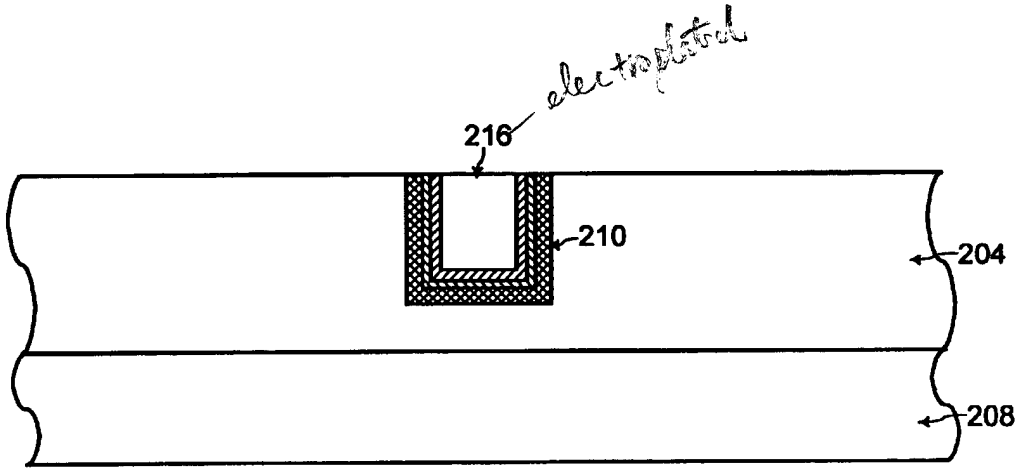


FIG. 12

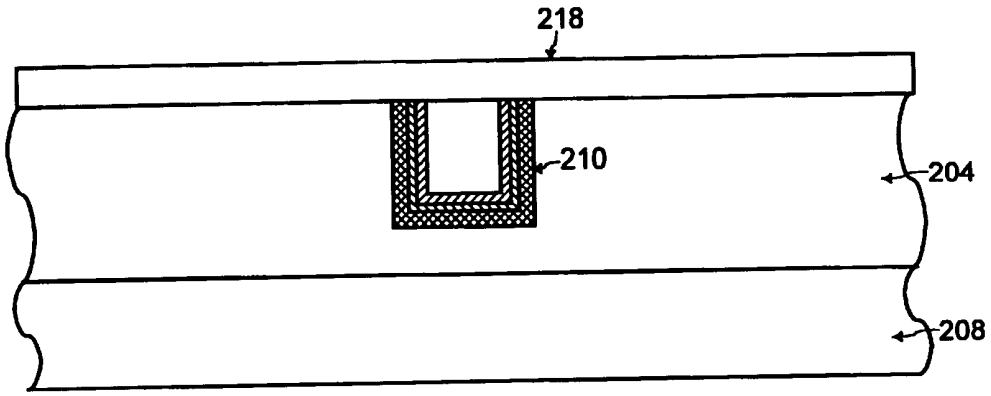


FIG. 13

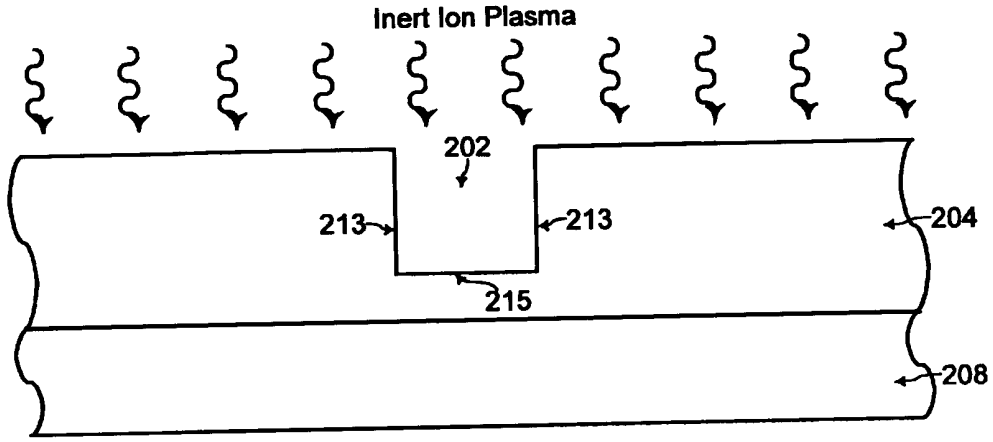


FIG. 14

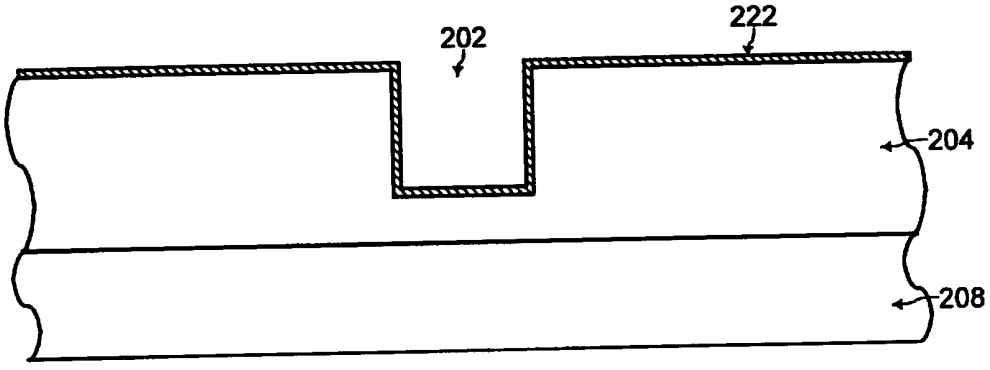


FIG. 15

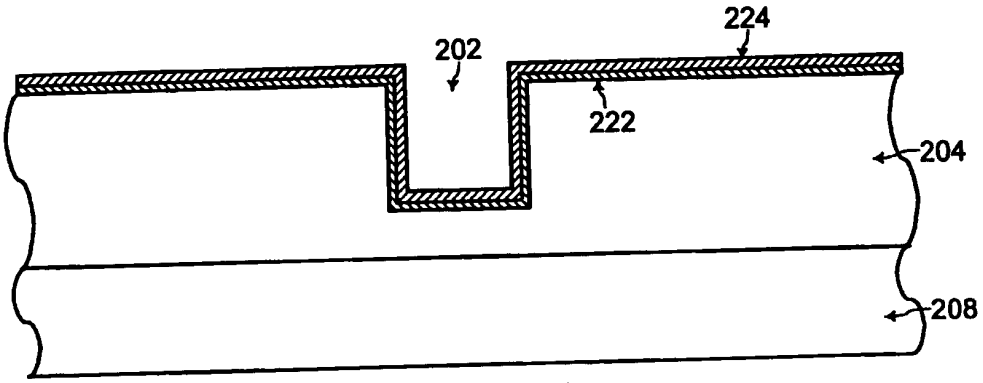


FIG. 16

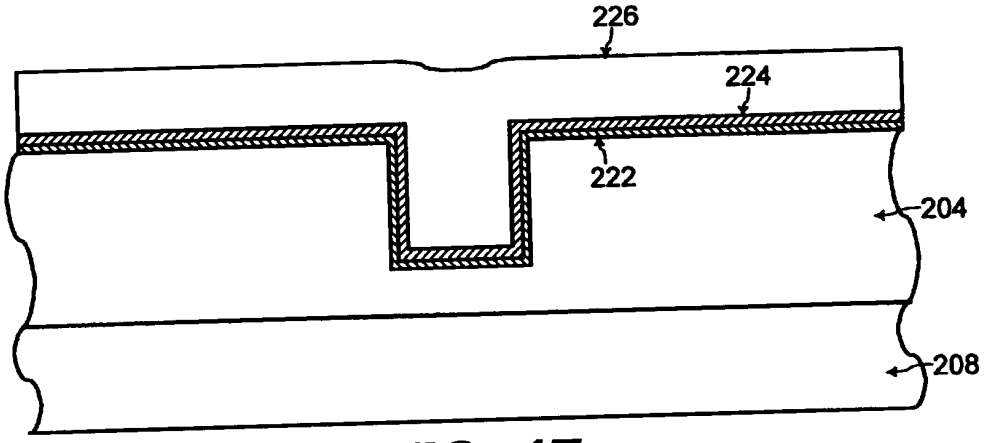


FIG. 17

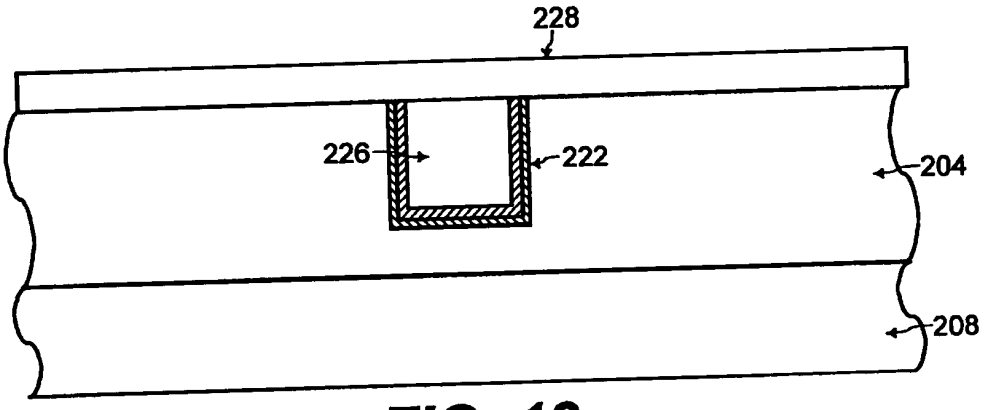


FIG. 18

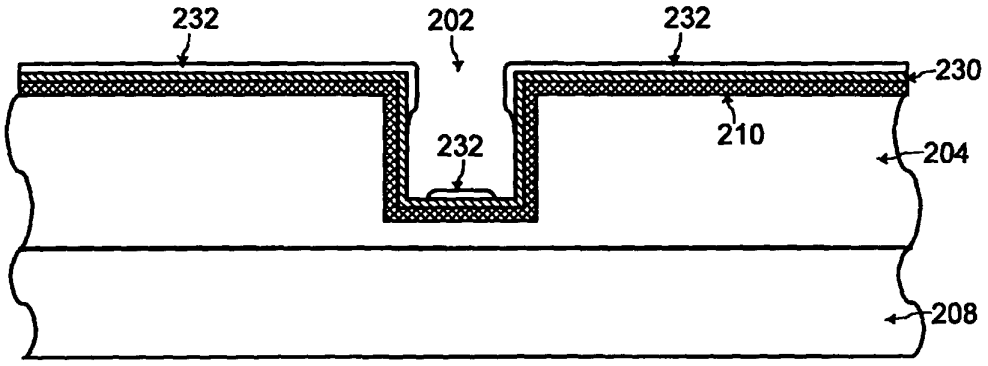


FIG. 19

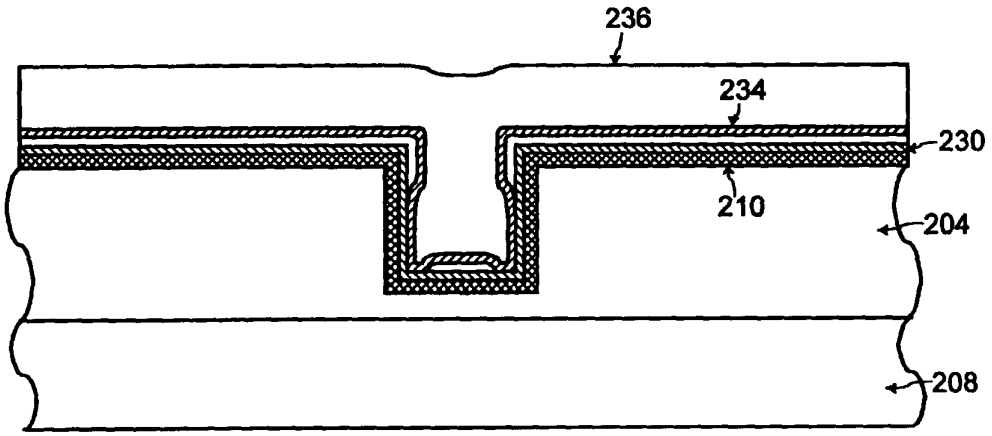


FIG. 20

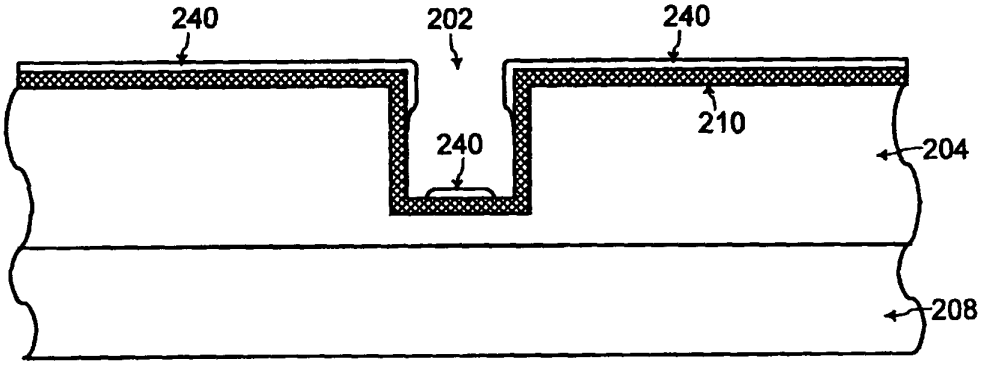


FIG. 21

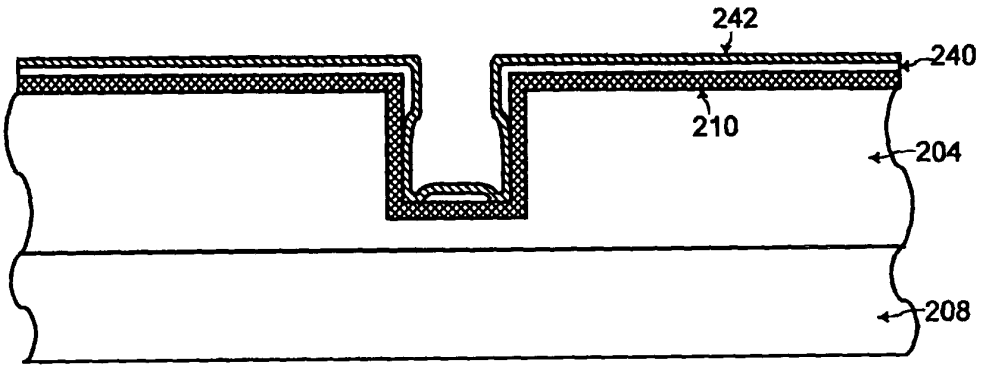


FIG. 22

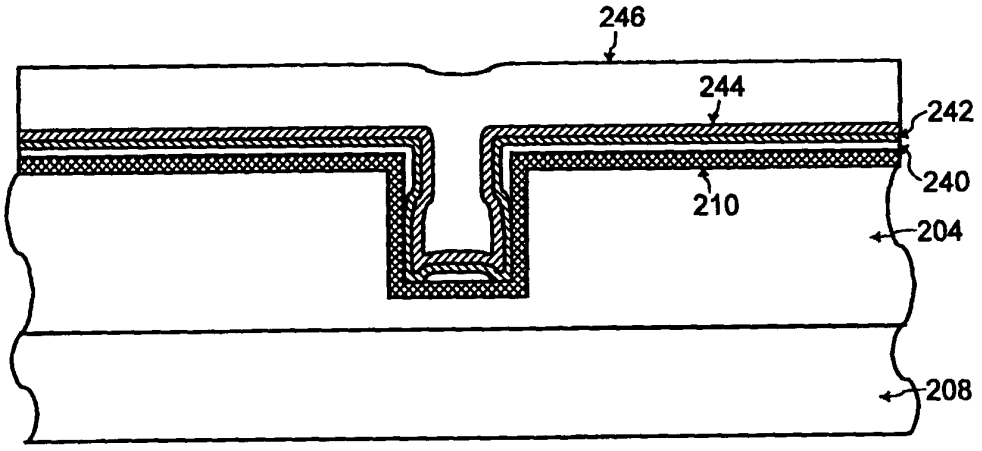


FIG. 23

DEPOSITING AN ADHESION SKIN LAYER AND A CONFORMAL SEED LAYER TO FILL AN INTERCONNECT OPENING

TECHNICAL FIELD

The present invention relates generally to fabrication of interconnect, such as copper interconnect for example, within an integrated circuit, and more particularly, to depositing an adhesion skin layer and a thin conformal seed layer for filling an interconnect opening to minimize electromigration and void formation within the interconnect.

BACKGROUND OF THE INVENTION

A long-recognized important objective in the constant advancement of monolithic IC (Integrated Circuit) technology is the scaling-down of IC dimensions. Such scaling-down of IC dimensions reduces area capacitance and is critical to obtaining higher speed performance of integrated circuits. Moreover, reducing the area of an IC die leads to higher yield in IC fabrication. Such advantages are a driving force to constantly scale down IC dimensions.

Thus far, aluminum has been prevalently used for metallization within integrated circuits. However, as the width of metal lines are scaled down to smaller submicron and even nanometer dimensions, aluminum metallization shows electromigration failure. Electromigration failure, which may lead to open and extruded metal lines, is now a commonly recognized problem. Moreover, as dimensions of metal lines further decrease, metal line resistance increases substantially, and this increase in line resistance may adversely affect circuit performance.

Given the concerns of electromigration and line resistance with smaller metal lines and vias, copper is considered a more viable metal for smaller metallization dimensions. Copper has lower bulk resistivity and potentially higher electromigration tolerance than aluminum. Both the lower bulk resistivity and the higher electromigration tolerance improve circuit performance.

Referring to FIG. **1**, a cross sectional view is shown of a copper interconnect **102** within a trench **104** formed in an insulating layer **106**. The copper interconnect **102** within the insulating layer **106** is formed on a semiconductor wafer **108** such as a silicon substrate as part of an integrated circuit. Because copper is not a volatile metal, copper cannot be easily etched away in a deposition and etching process as typically used for aluminum metallization. Thus, the copper interconnect **102** is typically formed by etching the trench **104** as an opening within the insulating layer **106**, and the trench **104** is then filled with copper typically by an electroplating process, as known to one of ordinary skill in the art of integrated circuit fabrication.

Unfortunately, copper is a mid-bandgap impurity in silicon and silicon dioxide. Thus, copper may diffuse easily into these common integrated circuit materials. Referring to FIG. **1**, the insulating layer **106** may be comprised of silicon dioxide or a low dielectric constant insulating material such as organic doped silica, as known to one of ordinary skill in the art of integrated circuit fabrication. The low dielectric constant insulating material has a dielectric constant that is lower than that of pure silicon dioxide (SiO_2) for lower capacitance of the interconnect, as known to one of ordinary skill in the art of integrated circuit fabrication.

Copper may easily diffuse into such an insulating layer **106**, and this diffusion of copper may degrade the performance of the integrated circuit. Thus, a diffusion barrier material **110** is deposited to surround the copper interconnect **102** within the insulating layer **106** on the sidewalls and the bottom wall of the copper interconnect **102**, as known to one of ordinary skill in the art of integrated circuit fabrication. The diffusion barrier material **110** is disposed between the copper interconnect **102** and the insulating layer **106** for preventing diffusion of copper from the copper interconnect **102** to the insulating layer **106** to preserve the integrity of the insulating layer **106**.

Further referring to FIG. **1**, an encapsulating layer **112** is deposited as a passivation layer to encapsulate the copper interconnect **102**, as known to one of ordinary skill in the art of integrated circuit fabrication. The encapsulating layer **112** is typically comprised of a dielectric such as silicon nitride, and copper from the copper interconnect **102** does not easily diffuse into such a dielectric of the encapsulating layer **112**.

Referring to FIG. **2**, typically for filling the trench **104** with copper, a diffusion barrier material **121** is deposited on the sidewalls and the bottom wall of the trench **104**. The diffusion barrier material **121** is similar to the diffusion barrier material **110** of FIG. **1**. A seed layer **122** of copper is deposited on the diffusion barrier material **121** at the sidewalls and the bottom wall of the trench **104**, and then copper is electroplated from the seed layer **122** to fill the trench **104** in an ECD (electrochemical deposition) process, as known to one of ordinary skill in the art of integrated circuit fabrication. The seed layer **122** of copper is typically deposited by a PVD (plasma-vapor-deposition) process as known to one of ordinary skill in the art of integrated circuit fabrication. With such a deposition process, referring to FIG. **2**, when the aspect ratio (defined as the depth to the width) of the trench **104** to be filled with copper is relatively large (i.e., greater than 5:1), the seed layer **122** that is deposited on the sidewalls and the bottom wall of the opening **104** may have a significant overhang **124** at the top corners of the interconnect opening **104**.

Referring to FIGS. **2** and **3**, when copper fill **126** is plated from the seed layer **122**, the copper that is plated from the overhang **124** may close off the top of the interconnect opening **104** before a center portion of the interconnect opening **104** is filled with copper to result in formation of a void **128** within the copper fill **126** toward the center of the interconnect opening **104**. Such a void **128** disadvantageously increases the resistance of the interconnect and may even contribute to electromigration failure of the interconnect.

Referring to FIG. **4**, to minimize the overhang **124** at the top corners of the interconnect opening **104**, the seed layer of copper **122** is deposited to be thinner. However, the deposition of the seed layer **122** is not perfectly conformal when the seed layer **122** is too thin (having a thickness of less than about 100 angstroms) when the conventional PVD (plasma-vapor-deposition) process for depositing the seed layer **122** is used. The seed layer **122** may be discontinuous and may not form at the sidewalls and the bottom corners of the interconnect opening **104**. However, it is desired for the copper fill to be plated from substantially all surfaces of the interconnect opening **104** including substantially the whole surface of the sidewalls and the bottom corners of the interconnect opening **104** to prevent void formation. Nevertheless, a thinner seed layer **122** is also desired to avoid formation of the overhang **124** for the interconnect opening **104** having high aspect ratio.

Referring to FIG. **5**, because the seed layer **122** is discontinuous when the seed layer **122** is too thin, a seed

enhancement layer **130** is formed on the seed layer **122**. The seed enhancement layer **130** is a thinner layer of copper (having a thickness of about 50 angstroms to about 500 angstroms). The seed enhancement layer **130** is formed by an ECD (electrochemical deposition) or a CVD (chemical-vapor-deposition) process instead of the conventional PVD (physical-vapor-deposition) process (for forming the seed layer **122**) such that the seed enhancement layer **130** is conformal to continuously cover substantially all exposed surfaces within the interconnect opening **104**. A copper fill **132** is then plated from the seed enhancement layer **130** and the seed layer **122**.

However, because the seed enhancement layer **130** is formed by an ECD (electrochemical deposition) or a CVD (chemical-vapor-deposition) process instead of the conventional PVD (physical-vapor-deposition) process for forming the seed layer **122**, the seed enhancement layer **130** does not adhere as well as the seed layer **122** to the underlying material of the diffusion barrier material **121** at the sidewalls and the bottom wall of the interconnect opening **104**, as known to one of ordinary skill in the art of integrated circuit fabrication. The seed layer **122** which is formed by the conventional PVD (physical-vapor-deposition) process adheres better to the underlying material of the insulating layer **106** at the sidewalls and the bottom wall of the interconnect opening **104**, as known to one of ordinary skill in the art of integrated circuit fabrication.

The poor adhesion of the seed enhancement layer **130** to the underlying material of the diffusion barrier material **121** at the sidewalls and the bottom wall of the interconnect opening **104** is more likely to result in disadvantageous electromigration failure of the interconnect. On the other hand, a relatively thick seed layer **122** has overhang **124** at the top corners of the interconnect opening having high aspect ratio which is more likely to result in disadvantageous void formation within the interconnect.

Thus, a mechanism is desired for filling an interconnect opening having high aspect ratio with minimized electromigration failure and minimized void formation.

SUMMARY OF THE INVENTION

Accordingly, in a general aspect of the present invention, for filling an interconnect opening having high aspect ratio, a thin adhesion skin layer including a metal alloy doping element is first deposited on the underlying material at the sidewalls and the bottom wall of the interconnect opening. A conformal seed layer such as the seed enhancement layer for example is deposited onto the thin adhesion skin layer, and the conductive fill is plated from the conformal seed layer.

In one aspect of the present invention, for filling an interconnect opening within an insulating layer on a semiconductor wafer, an adhesion skin layer is deposited conformally onto an underlying material comprised of one of a barrier material or a dielectric material at sidewalls and a bottom wall of the interconnect opening. The adhesion skin layer includes a metal alloy doping element. A conformal seed layer is deposited onto the adhesion skin layer using a conformal deposition process, such as an ECD (electrochemical deposition) or a CVD (chemical-vapor-deposition) process, for depositing a conformal seed layer. The adhesion skin layer promotes adhesion of the conformal seed layer to the underlying material at the sidewalls and the bottom wall of the interconnect opening. The interconnect opening is filled with a conductive material grown from the conformal seed layer.

The present invention may be used to particular advantage when the conductive material filling the interconnect opening is comprised of substantially pure copper and when the conformal seed layer is comprised of substantially pure copper having a thickness in a range of from about 50 angstroms to about 500 angstroms. In addition, the present invention may be used to particular advantage when the adhesion skin layer is comprised of one of substantially pure zirconium, substantially pure tin, substantially pure zinc, substantially pure indium, or a copper alloy including one of zirconium, tin, zinc or indium having a concentration in copper of from about 0.01 atomic percent to about 10 atomic percent. The adhesion skin layer has a thickness in a range of from about 3 angstroms to about 100 angstroms in one embodiment of the present invention.

When a low deposition temperature below about 25° Celsius is used for depositing the adhesion skin layer, a thinner but yet continuous adhesion skin layer may be achieved. In addition, the underlying material is bombarded with an inert ion plasma to achieve a thinner but yet continuous adhesion skin layer. Furthermore, a thermal anneal process is performed by heating the conformal seed layer and the adhesion skin layer to further enhance the adhesion of the conformal seed layer to the underlying material.

In this manner, the adhesion skin layer promotes adhesion of the conformal seed layer to the underlying material to minimize electromigration failure of the interconnect. In addition, the seed layer formed by conventional PVD (physical-vapor-deposition) processes is avoided with the present invention. Instead, the relatively thin adhesion skin layer (having a thickness of about 3–100 angstroms) and the relatively thin conformal seed layer (having a thickness of about 50–500 angstroms) are used for plating the conductive fill. With such relatively thin layers, an interconnect opening having a high aspect ratio is filled with minimized void formation.

These and other features and advantages of the present invention will be better understood by considering the following detailed description of the invention which is presented with the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows a cross-sectional view of a copper interconnect formed by copper filling a trench within an insulating layer, according to the prior art;

FIG. **2** shows a cross-sectional view of a seed layer of copper deposited on a diffusion barrier material at the sidewalls and the bottom wall of an interconnect opening for illustrating the formation of an overhang of the seed layer at the top corners of the interconnect opening when a relatively thick seed layer is deposited, according to the prior art;

FIG. **3** shows a cross-sectional view of a copper fill plated from the seed layer of FIG. **2** for illustrating the formation of a void within the copper fill from the overhang of the seed layer of FIG. **2**, according to the prior art;

FIG. **4** shows a cross-sectional view of a relatively thin seed layer of copper deposited on the sidewalls and bottom wall of an interconnect opening for illustrating the discontinuity of the seed layer, according to the prior art;

FIG. **5** shows a cross-sectional view of the relatively thin seed layer of copper of FIG. **4** with a conformal seed layer deposited on any exposed surfaces within the interconnect opening, according to the prior art;

FIGS. **6**, **7**, **8**, **9**, **10**, **11**, **12**, and **13** show cross-sectional views for formation of an interconnect to illustrate process

steps for depositing an adhesion skin layer and a conformal seed layer onto a diffusion barrier material for plating the conductive fill of the interconnect, to minimize electromigration failure and void formation according to one embodiment of the present invention;

FIGS. **14**, **15**, **16**, **17**, and **18** show cross-sectional views for formation of an interconnect to illustrate process steps for depositing an adhesion skin layer and a conformal seed layer onto an insulating material of the insulating layer for plating the conductive fill of the interconnect, to minimize electromigration failure and void formation according to another embodiment of the present invention;

FIGS. **19** and **20** show cross-sectional views for formation of an interconnect to illustrate process steps for depositing a non-conformal seed layer between the adhesion skin layer and the conformal seed layer, according to a further embodiment of the present invention; and

FIGS. **21**, **22**, and **23** show cross-sectional views for formation of an interconnect to illustrate process steps for depositing a non-conformal seed layer before depositing the adhesion skin layer and the conformal seed layer, according to another embodiment of the present invention.

The figures referred to herein are drawn for clarity of illustration and are not necessarily drawn to scale. Elements having the same reference number in FIGS. **1**, **2**, **3**, **4**, **5**, **6**, **7**, **8**, **9**, **10**, **11**, **12**, **13**, **14**, **15**, **16**, **17**, **18**, **19**, **20**, **21**, **22**, and **23** refer to elements having similar structure and function.

DETAILED DESCRIPTION

The present invention is described for formation of copper interconnect. However, the present invention may be practiced for minimizing electromigration failure and void formation with conductive fill of other types of interconnects, as would be apparent to one of ordinary skill in the art of integrated circuit fabrication from the description herein.

Referring to FIG. **6**, for forming an interconnect such as copper interconnect, an interconnect opening **202** such as a trench line is formed within an insulating layer **204** on a semiconductor wafer **208** as part of an integrated circuit, as known to one of ordinary skill in the art of integrated circuit fabrication. Typically, the semiconductor wafer **208** is comprised of silicon (Si), and the insulating layer **204** is comprised of silicon dioxide (SiO_2) or a low dielectric constant insulating material such as organic doped silica, as known to one of ordinary skill in the art of integrated circuit fabrication.

Copper interconnect is desirable for metallization within an integrated circuit with scaled down dimensions because copper has lower bulk resistivity and potentially higher electromigration tolerance than aluminum. However, because copper is not a volatile metal, copper cannot be easily etched away in a deposition and etching process as typically used for aluminum metallization. Thus, copper interconnect is typically formed by etching the interconnect opening **202** within the insulating layer **204** and then filling the interconnect opening **202** with copper fill.

Referring to FIG. **7**, a diffusion barrier material **210** is deposited on the exposed surfaces of the insulating layer **204** including the sidewalls **213** and the bottom wall **215** of the interconnect opening **202**. The diffusion barrier material **210** prevents diffusion of copper to be filled within the interconnect opening **202** into the surrounding insulating layer **204**. The diffusion barrier material **210** may be a diffusion barrier metal or a diffusion barrier dielectric. Such diffusion barrier materials and processes for deposition of such diffusion barrier materials are known to one of ordinary skill in the art of integrated circuit fabrication.

Unfortunately, copper is a mid-bandgap impurity in silicon and silicon dioxide. Thus, copper may diffuse easily into these common integrated circuit materials. Referring to FIG. **7**, the insulating layer **204** is typically comprised of silicon dioxide or a low dielectric constant insulating material such as organic doped silica, as known to one of ordinary skill in the art of integrated circuit fabrication, especially when the semiconductor wafer **208** is a silicon substrate.

Copper may easily diffuse into the insulating layer **204**, and this diffusion of copper may degrade the performance of the integrated circuit. Thus, the diffusion barrier material **210** is deposited to surround the copper to be filled within the interconnect opening **202**. The diffusion barrier material **210** prevents diffusion of copper to filled within the interconnect opening **202** to the insulating layer **204** to preserve the integrity of the insulating layer **204**.

Referring to FIG. **8**, exposed surfaces of the diffusion barrier material **210** are bombarded with an inert ion plasma in an isotropic plasma process (i.e., a plasma process using high process pressure of greater than about 10 milliTorr and a low voltage bias for an ion energy that is less than about 100 eV). The inert ion plasma is comprised of argon or helium, and preferably argon when the diffusion barrier material **210** is comprised of tantalum, titanium, tungsten, or these elements in a compound form with nitrogen, carbon, or silicon. Such plasma processes are known to one of ordinary skill in the art of integrated circuit fabrication. After the inert ion plasma bombards the exposed surfaces of the diffusion barrier material **210**, the exposed surfaces of the diffusion barrier material **210** are roughened.

Referring to FIG. **9**, an adhesion skin layer **212** is deposited onto the underlying material of the diffusion barrier material **210**. The adhesion skin layer **212** includes a metal alloy doping element. In one embodiment of the present invention, the adhesion skin layer **212** is a copper alloy including the metal alloy doping element of zirconium, tin, zinc, or indium having a concentration in copper of from about 0.01 atomic percent to about 10 atomic percent. In another embodiment of the present invention, the adhesion skin layer **212** is comprised of the substantially pure metal alloy doping element such as substantially pure zirconium, substantially pure tin, substantially pure zinc, or substantially pure indium.

In either case, in one embodiment of the present invention, the adhesion skin layer **212** is relatively thin, having a thickness in a range of from about 3 angstroms to about 100 angstroms. Referring to FIGS. **8** and **9**, when the exposed surfaces of the diffusion barrier material **210** are roughened with bombardment by inert ion plasma, the adhesion skin layer **212** has a higher nucleation density to be thinner and yet substantially continuous. In addition, a relatively low deposition temperature of less than about 25° Celsius is used in a preferred embodiment of the present invention for forming the adhesion skin layer **212** with higher nucleation density such that the adhesion skin layer **212** may be thinner and yet substantially continuous. Such higher nucleation density results in smaller grain size within the adhesion skin layer **212** and thus in a smoother adhesion skin layer **212**.

Processes, such as CVD (chemical-vapor-deposition) or ALD (atomic layer deposition) processes, which are conformal deposition processes, for forming the adhesion skin layer **212** comprised of substantially pure metal alloy doping element are known to one of ordinary skill in the art of integrated circuit fabrication. The patent application with Ser. No. 09/845,616 having title

Formation of Alloy Material using Alternating Depositions of a Layer of Alloy Doping Element and a Layer of Bulk Material, and having the same inventors and filed concurrently herewith, describes a process for forming the adhesion skin layer **212** comprised of an alloy material such as copper alloy. This patent application with Ser. No. 09/845,616 is in its entirety incorporated herein by reference.

Referring to FIG. **10**, a conformal seed layer **214** is deposited onto the adhesion skin layer **212** using a conformal deposition process. For example, the conformal seed layer **214** is deposited using a deposition process for depositing the seed enhancement layer **130** in FIG. **5**. In one embodiment of the present invention, the conformal seed layer **214** is comprised of substantially pure copper having a thickness in a range of from about 50 angstroms to about 500 angstroms. Processes, such as ECD (electrochemical deposition) processes and CVD (chemical-vapor-deposition) processes, for depositing such a thin conformal seed layer **214** are different from processes, such as conventional PVD (physical-vapor-deposition) processes, for depositing the thicker seed layer **122** of FIGS. **2**, **4**, and **5** of the prior art, as known to one of ordinary skill in the art of integrated circuit fabrication.

The adhesion skin layer **212** having the metal alloy doping element promotes adhesion between the conformal seed layer **214** and the diffusion barrier material **210**. In one embodiment of the present invention, after deposition of the conformal seed layer **214** on the adhesion skin layer **212**, a thermal anneal is performed by heating the conformal seed layer **214** and the adhesion skin layer **212** at a temperature of from about 100° Celsius to about 400° Celsius for a time period of from about 2 seconds to about 60 minutes. Such a thermal anneal process further promotes adhesion between the conformal seed layer **214** and the diffusion barrier material **210** by the adhesion skin layer **212** having the metal alloy doping element.

Referring to FIG. **11**, the interconnect opening **202** is filled with a conductive material **216** grown from the conformal seed layer **214**. For example, when the conformal seed layer **214** is comprised of substantially pure copper, the conductive material **216** is comprised of substantially pure copper electroplated from the conformal seed layer **214**, according to one embodiment of the present invention. Electroplating processes for filling the interconnect opening **202** with copper **216** grown from the conformal seed layer **214** are known to one of ordinary skill in the art of integrated circuit fabrication.

Referring to FIG. **12**, any of the conductive material **216**, the conformal seed layer **214**, and the adhesion skin layer **212** on the insulating layer **204** surrounding the interconnect opening **202** is polished away to expose the insulating layer **204** such that the interconnect is contained within the interconnect opening **202**. Processes, such as CMP (chemical mechanical polishing) processes are known to one of ordinary skill in the art of integrated circuit fabrication.

Referring to FIG. **13**, a layer of bulk passivation material **218** is deposited on the insulating layer **204** and on top of the interconnect within the interconnect opening **202**. The bulk passivation material **218** may be comprised of one of silicon oxynitride (SiON), silicon nitride (SiN), and a silicon carbide (SiC) film doped with hydrogen, and copper does not easily diffuse through such a bulk passivation material **218**. Processes for depositing such bulk passivation material **218** are known to one of ordinary skill in the art of integrated circuit fabrication.

In this manner, the adhesion skin layer **212** promotes adhesion between the conformal seed layer **214** and the underlying diffusion barrier material **210** to minimize electromigration failure of the interconnect. In addition, the prior art seed layer formed by conventional PVD (physical-vapor-deposition) processes is avoided with the present invention. Instead, the relatively thin adhesion skin layer **212** (having a thickness of about 3–100 angstroms) and the relatively thin conformal seed layer **214** (having a thickness of about 50–500 angstroms) are used for plating the conductive material **216**. With such relatively thin layers **212** and **214**, an interconnect opening having high aspect ratio is filled with minimized void formation.

Referring to FIG. **14**, in an alternative embodiment of the present invention, the adhesion skin layer and the conformal seed layer are formed on the dielectric material of the insulating layer **204** when a diffusion barrier material is not used. For example, with advancement of technology for dielectric material, the insulating layer **204** may be comprised of an insulating material that is impervious to copper diffusion such that a diffusion barrier material is not used. Alternatively, the insulating material **204** may be comprised of silicon dioxide or a low dielectric constant insulating material such as organic doped silica.

Referring to FIG. **14**, exposed surfaces of the insulating layer **204** are bombarded with an inert ion plasma in an isotropic plasma process (i.e., a plasma process using high process pressure of greater than about 10 milliTorr and a low voltage bias for an ion energy that is less than about 100 eV). The inert ion plasma is comprised of argon or helium, and preferably helium for the insulating material of the insulating layer **204**. Such plasma processes are known to one of ordinary skill in the art of integrated circuit fabrication. After the inert ion plasma bombards the exposed surfaces of the insulating layer **204**, the exposed surfaces of the insulating layer **204** including the sidewalls **213** and the bottom wall **215** are roughened.

Referring to FIG. **15**, an adhesion skin layer **222**, similar to the adhesion skin layer **212** of FIG. **9**, is conformally deposited onto the underlying material of the insulating layer **204**. The adhesion skin layer **222** includes a metal alloy doping element. In one embodiment of the present invention, the adhesion skin layer **222** is a copper alloy including the metal alloy doping element of zirconium, tin, zinc, or indium having a concentration in copper of from about 0.01 atomic percent to about 10 atomic percent. In another embodiment of the present invention, the adhesion skin layer **222** is comprised of the substantially pure metal alloy doping element such as substantially pure zirconium, substantially pure tin, substantially pure zinc, or substantially pure indium.

In either case, in one embodiment of the present invention, the adhesion skin layer **222** is relatively thin having a thickness in a range of from about 3 angstroms to about 100 angstroms. Referring to FIGS. **14** and **15**, when the exposed surfaces of the insulating layer **204** are roughened with bombardment by inert ion plasma, the adhesion skin layer **222** may be thinner and yet substantially continuous. In addition, a relatively low deposition temperature of less than about 25° Celsius is used in a preferred embodiment of the present invention for forming the adhesion skin layer **222** with higher nucleation density such that the adhesion skin layer **222** may be thinner and yet substantially continuous.

Processes, such as CVD (chemical-vapor-deposition) or ALD (atomic layer deposition) processes, which are conformal deposition processes, for forming the adhesion skin layer **222** comprised of substantially pure metal alloy doping element are known to one of ordi-

nary skill in the art of integrated circuit fabrication. The patent application with Ser. No. 09/845,616 having title Formation of Alloy Material using Alternating Depositions of a Layer of Alloy Doping Element and a Layer of Bulk Material, and having the same inventors and filed concurrently herewith, describes a process for forming the adhesion skin layer **222** comprised of an alloy material such as copper alloy. This patent application with Serial No. 09/845,616 is in its entirety incorporated herein by reference.

Referring to FIG. **16**, a conformal seed layer **224** is deposited onto the adhesion skin layer **222** using a conformal deposition process. For example, the conformal seed layer **224** is deposited using a deposition process for depositing the seed enhancement layer **130** in FIG. **5**. In one embodiment of the present invention, the conformal seed layer **224** is comprised of substantially pure copper having a thickness in a range of from about 50 angstroms to about 500 angstroms. Processes, such as ECD (electrochemical deposition) processes and CVD (chemical-vapor-deposition) processes, for depositing such a thin conformal seed layer **224** are different from processes, such as conventional PVD (physical-vapor-deposition) processes, for depositing the thicker seed layer **122** of FIGS. **2**, **4**, and **5** of the prior art, as known to one of ordinary skill in the art of integrated circuit fabrication.

The adhesion skin layer **222** having the metal alloy doping element promotes adhesion between the conformal seed layer **224** and the insulating layer **204**. In one embodiment of the present invention, after deposition of the conformal seed layer **224** on the adhesion skin layer **222**, a thermal anneal is performed by heating the conformal seed layer **224** and the adhesion skin layer **222** at a temperature of from about 100° Celsius to about 400° Celsius for a time period of from about 2 seconds to about 60 minutes. Such a thermal anneal process further promotes adhesion between the conformal seed layer **224** and the insulating layer **204** by the adhesion skin layer **222** having the metal alloy doping element.

Referring to FIG. **17**, the interconnect opening **202** is filled with a conductive material **226** grown from the conformal seed layer **224**. For example, when the conformal seed layer **224** is comprised of substantially pure copper, the conductive material **226** is comprised of substantially pure copper electroplated from the conformal seed layer **224**, according to one embodiment of the present invention. Electroplating processes for filling the interconnect opening **202** with copper **226** grown from the conformal seed layer **224** are known to one of ordinary skill in the art of integrated circuit fabrication.

Referring to FIG. **18**, any of the conductive material **226**, the conformal seed layer **224**, and the adhesion skin layer **222** on the insulating layer **204** surrounding the interconnect opening **202** is polished away to expose the insulating layer **204** such that the interconnect is contained within the interconnect opening **202**. Processes, such as CMP (chemical mechanical polishing) processes are known to one of ordinary skill in the art of integrated circuit fabrication.

Further referring to FIG. **18**, a layer of bulk passivation material **228** is deposited on the insulating layer **204** and on top of the interconnect within the interconnect opening **202**. The bulk passivation material **228** may be comprised of one of silicon oxynitride (SiON), silicon nitride (SiN), and a silicon carbide (SiC) film doped with hydrogen, and copper does not easily diffuse through such a bulk passivation material **228**. Processes for depositing such bulk passivation material **228** are known to one of ordinary skill in the art of integrated circuit fabrication.

In this manner, the adhesion skin layer **222** promotes adhesion between the conformal seed layer **224** to the underlying insulating material of the insulating layer **204** to minimize electromigration failure of the interconnect. In addition, the prior art seed layer formed by conventional PVD (physical-vapor-deposition) processes is avoided with the present invention. Instead, the relatively thin adhesion skin layer **222** (having a thickness of about 3–100 angstroms) and the relatively thin conformal seed layer **224** (having a thickness of about 50–500 angstroms) are used for plating the conductive material **226**. With such relatively thin layers **222** and **224**, an interconnect opening having a high aspect ratio is filled with minimized void formation.

Referring to FIG. **19**, in a further embodiment of the present invention, an adhesion skin layer **230** is deposited on the underlying diffusion barrier material **210**, and a non-conformal seed layer **232** is deposited on the adhesion skin layer **230**. The adhesion skin layer **230** is similar to the adhesion skin layer **212** of FIG. **6** or **222** of FIG. **15**, as described herein. The non-conformal seed layer **232** is similar to the non-conformal seed layer **122** of FIG. **4** as described herein and is relatively thin (having a thickness of less than about 100 angstroms). Similar to the non-conformal seed layer **122** of FIG. **4**, the non-conformal seed layer **232** of FIG. **19** is deposited by a non-conformal deposition process such as a PVD (plasma-vapor-deposition) process.

Referring to FIG. **20**, a conformal seed layer **234** is deposited on the non-conformal seed layer **232** and on portions of the adhesion skin layer **230** not having the non-conformal seed layer **232** deposited thereon. The conformal seed layer **234** is similar to the conformal seed layer **214** of FIG. **10** or **224** of FIG. **16**, as described herein. Further referring to FIG. **20**, a conductive material **236** is plated from the conformal seed layer **234**. The conductive material **236** is similar to the conductive material **216** of FIG. **11** or **226** of FIG. **17**, as described herein. This embodiment of depositing the non-conformal seed layer **232** between the adhesion skin layer **230** and the conformal seed layer **234** may also be practiced when the underlying material is the dielectric material of the insulating layer **204**, as would be apparent to one of ordinary skill in the art of integrated circuit fabrication from the description herein.

Referring to FIG. **21**, in another embodiment of the present invention, a non-conformal seed layer **240** is initially deposited on the underlying diffusion barrier material **210**. The non-conformal seed layer **240** is similar to the non-conformal seed layer **122** of FIG. **4** as described herein and is relatively thin (having a thickness of less than about 100 angstroms). Similar to the non-conformal seed layer **122** of FIG. **4**, the non-conformal seed layer **232** of FIG. **21** is deposited by a non-conformal deposition process such as a PVD (plasma-vapor-deposition) process.

Referring to FIG. **22**, an adhesion skin layer **242** is deposited on the non-conformal seed layer **240** and on portions of the underlying diffusion barrier material **210** not having the non-conformal seed layer **240** deposited thereon. The adhesion skin layer **242** is similar to the adhesion skin layer **212** of FIG. **6** or **222** of FIG. **15**, as described herein. Referring to FIG. **23**, a conformal seed layer **244** is deposited on the adhesion skin layer **242**. The conformal seed layer **244** is similar to the conformal seed layer **214** of FIG. **10** or **224** of FIG. **16**, as described herein. Further referring to FIG. **23**, a conductive material **246** is plated from the conformal seed layer **244**. The conductive material **246** is similar to the conductive material **216** of FIG. **11** or **226** of FIG. **17**, as described herein. This embodiment of depositing

the non-conformal seed layer **232** before depositing the adhesion skin layer **230** and the conformal seed layer **234** may also be practiced when the underlying material is the dielectric material of the insulating layer **204**, as would be apparent to one of ordinary skill in the art of integrated circuit fabrication from the description herein.

The foregoing is by way of example only and is not intended to be limiting. For example, the present invention is described for formation of copper interconnect. However, the present invention may be practiced for minimizing electromigration failure and void formation within conductive fill of other types of interconnects, as would be apparent to one of ordinary skill in the art of integrated circuit fabrication from the description herein. Any materials or dimensions specified herein are by way of example only. In addition, the present invention may be practiced with the adhesion skin layer **222** being conformal or not conformal and with the adhesion skin layer **222** being continuous or not continuous, as would be apparent to one of ordinary skill in the art of integrated circuit fabrication from the description herein. On the other hand, the conformal skin layer **214** or **224** is deposited in a conformal deposition process.

Furthermore, as will be understood by those skilled in the art, the structures described herein may be made or used in the same way regardless of their position and orientation. Accordingly, it is to be understood that terms and phrases such as "top," "bottom," and "sidewall" as used herein refer to relative location and orientation of various portions of the structures with respect to one another, and are not intended to suggest that any particular absolute orientation with respect to external objects is necessary or required. The present invention is limited only as defined in the following claims and equivalents thereof.

We claim:

1. A method for filling an interconnect opening of an integrated circuit, said interconnect opening being with an insulating layer on a semiconductor wafer, the method including the steps of:

A. depositing an adhesion skin layer onto an underlying comprised of one of a barrier material or a dielectric at sidewalls and a bottom wall of said interconnect opening, wherein said adhesion skin layer includes a metal allow doping element;

B. depositing a conformal seed layer onto said adhesion skin layer using conformal deposition process;

wherein said conformal seed layer is comprised of a pure bulk element, and wherein said adhesion skin layer is an alloy comprised of said metal allow doping element and said pure bulk element also comprising said conformal seed layer with said metal allow doping element doping said pure bulk element within said adhesion skin layer;

and wherein said adhesion skin layer promotes adhesion of said conformal seed layer to said underlying material at said sidewalls and said bottom wall of said interconnect opening; and

C. filling said interconnect opening with a conductive material grown from said conformal seed layer that is comprised of said pure bulk element.

2. The method of claim **1**, further including the step of:

depositing a layer of non-conformal seed layer on portions of said adhesion skin layer, after said step A and before said step B;

wherein said conformal seed layer deposited in said step B is deposited on said non-conformal seed layer and on exposed portions of said adhesion skin layer not having said non-conformal seed layer deposited thereon.

3. The method of claim **1**, further including the step of:

depositing a layer of non-conformal seed layer on portions of said underlying material, before said step A;

wherein said adhesion skin layer deposited in said step A is deposited on said non-conformal seed layer and on exposed portions of said underlying material not having said non-conformal seed layer deposited thereon.

4. The method of claim **1**, wherein said adhesion skin layer is deposited using a conformal deposition process.

5. The method of claim **1**, wherein said underlying material at said sidewalls and said bottom wall of said interconnect opening is a diffusion barrier material.

6. The method of claim **1**, wherein said underlying material at said sidewalls and said bottom wall of said interconnect opening is an insulating material of said insulating layer that is comprised of a low dielectric constant material having a dielectric constant that is lower than silicon dioxide (SiO_2).

7. The method of claim **1**, further including the step of:

performing a thermal anneal after said step B and before said step C by heating said conformal seed layer and said adhesion skin layer at a temperature of from about 100° Celsius to about 400° Celsius for a time period of from about 2 seconds to about 60 minutes.

8. The method of claim **1**, further including the step of:

bombarding said underlying material at said sidewalls and said bottom wall of said interconnect opening with inert ion plasma, before said step A.

9. The method of claim **1**, further including the steps of:

polishing away any of said conductive material, said conformal seed layer, and said adhesion skin layer on said insulating layer surrounding said interconnect opening to expose said insulating layer such that said conductive material is contained within said interconnect opening; and

depositing a layer of bulk passivation material on said insulating layer and on top of said filled interconnect opening to encapsulate said interconnect opening.

10. The method of claim **1**, wherein said conductive material filling said interconnect opening in said step C is comprised of substantially pure copper.

11. The method of claim **10**, wherein said conformal seed layer is comprised of substantially pure copper having a thickness in a range of from about 50 angstroms to about 500 angstroms.

12. The method of claim **11**, wherein said conformal seed layer is deposited using one of an electro-chemical plating process or a CVD (chemical-vapor-deposition) process.

13. The method of claim **11**, wherein said adhesion skin layer is comprised of a copper alloy including said metal alloy doping element comprising one of zirconium, tin, zinc, or indium having a concentration in copper of from about 0.01 atomic percent to about 10 atomic percent.

14. The method of claim **13**, wherein said adhesion skin layer has a thickness in a range of from about 3 angstroms to about 100 angstroms.

15. The method of claim **14**, wherein said adhesion skin layer is deposited by one of a CVD (chemical-vapor-deposition) process or an ALD (atomic layer deposition) process.

16. The method of claim **15**, wherein said adhesion skin layer is deposited using a deposition temperature below about 25° Celsius.

17. A method for filling an interconnect opening of an integrated circuit with copper, said interconnect opening being within an insulating layer on a semiconductor wafer, the method including the sequential steps of:

A. bombarding an underlying material at sidewalls and a bottom wall of said interconnect opening with inert ion plasma formed from one of argon or helium; wherein said underlying material is comprised of one a diffusion barrier material deposited on said sidewalls and said bottom wall of said interconnect opening or an insulating material of said insulating layer that is comprised of a low dielectric constant material having a dielectric constant that is lower than silicon dioxide (SiO_2) when a barrier layer is not deposited on said sidewalls and said bottom wall of said interconnect opening;

B. depositing conformally an adhesion skin layer onto said underlying material at said sidewalls and said bottom wall of said interconnect opening;

wherein said adhesion skin layer is comprised of a copper alloy including one of zirconium, tin, zinc or indium having a concentration in copper of from about 0.01 atomic percent to about 10 atomic percent, said adhesion skin layer having a thickness in a range of from about 3 angstroms to about 100 angstroms;

and wherein said adhesion skin layer is deposited by one of a CVD (chemical-vapor-deposition) process or an ALD (atomic layer deposition) process, using a deposition temperature below about 25° Celsius;

C. depositing a conformal seed layer onto said adhesion skin layer using a conformal deposition process;

wherein said adhesion skin layer promotes adhesion of said conformal seed layer to said underlying material at said sidewalls and said bottom wall of said interconnect opening;

wherein said conformal seed layer is comprised of a pure bulk element, and wherein said adhesion skin layer is an alloy comprised of said metal alloy doping element and said pure bulk element also comprising said conformal seed layer with said metal alloy doping element doping said pure bulk element within said adhesion skin layer, and wherein said conformal seed layer is comprised of substantially pure copper having a thickness in a range of from about 50 angstroms to about 500 angstroms;

and wherein said conformal seed layer is deposited using one of an electro-chemical plating process or a CVD (chemical-vapor-deposition) process;

D. performing a thermal anneal by heating said conformal seed layer and said adhesion skin layer at a temperature of from about 100° Celsius to about 400° Celsius for a time period of from about 2 seconds to about 60 minutes;

E. filling said interconnect opening with a conductive material of substantially pure copper grown from said conformal seed layer that is comprised of said pure bulk element;

F. polishing away any of said conductive material, said conformal seed layer, and said adhesion skin layer on said insulating layer surrounding said interconnect opening to expose said insulating layer such that said conductive material is contained within said interconnect opening; and

G. depositing a layer of bulk passivation material on said insulating layer and on top of said filled interconnect opening to encapsulate said interconnect opening.

* * * * *

US006515368B1

(12) **United States Patent**
Lopatin et al.

(10) **Patent No.: US 6,515,368 B1**
(45) **Date of Patent: Feb. 4, 2003**

(54) **SEMICONDUCTOR DEVICE WITH COPPER-FILLED VIA INCLUDES A COPPER-ZINC/ ALLOY FILM FOR REDUCED ELECTROMIGRATION OF COPPER**

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(73) Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, CA (US)

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(21) Appl. No.: **10/016,410**

(22) Filed: **Dec. 7, 2001**

(51) **Int. Cl.**[7] **H01L 23/532**
(52) **U.S. Cl.** **257/762**; 257/751; 257/752; 257/767; 257/775
(58) **Field of Search** 251/751, 752, 251/758, 760, 761, 762, 764, 767, 775

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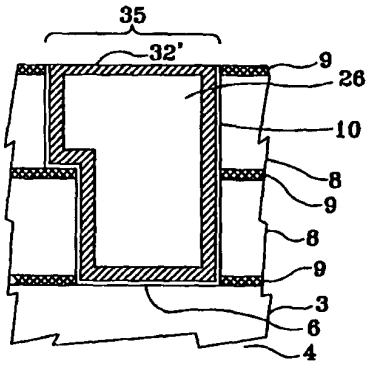
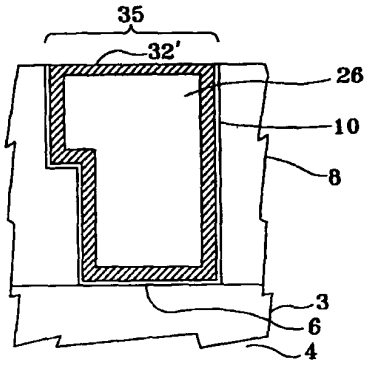
Primary Examiner—Carl Whitehead, Jr.
Assistant Examiner—Stephen W. Smoot
(74) *Attorney, Agent, or Firm*—LaRiviere, Grubman & Payne, LLP

(57) **ABSTRACT**

A method of reducing electromigration in copper interconnect lines by restricting Cu-diffusion pathways along a Cu surface via doping the Cu surface with Zn from an interim copper-zinc alloy (Cu—Zn) thin film electroplated on the copper (Cu) surface from a stable chemical solution, and controlling the Zn-doping thereof, which also improves interconnect reliability and corrosion resistance, and a semiconductor device thereby formed. The method involves using interim reduced-oxygen Cu—Zn alloy thin films for forming an encapsulated dual-inlaid interconnect structure. The films are formed by electroplating a Cu surface via by electroplating, the Cu surface in a unique chemical solution containing salts of Zn and Cu, their complexing agents, a pH adjuster, and surfactants; and annealing the interim electroplated Cu—Zn alloy thin films and a Cu-fill; and planarizing the interconnect structure.

10 Claims, 5 Drawing Sheets





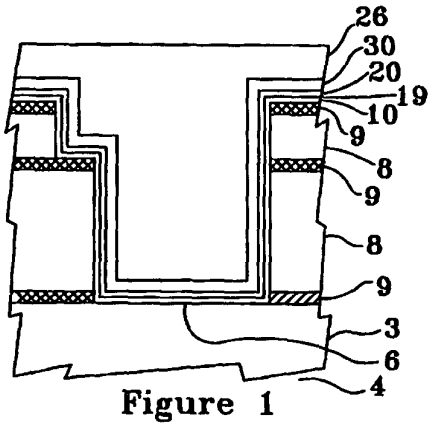


Figure 1

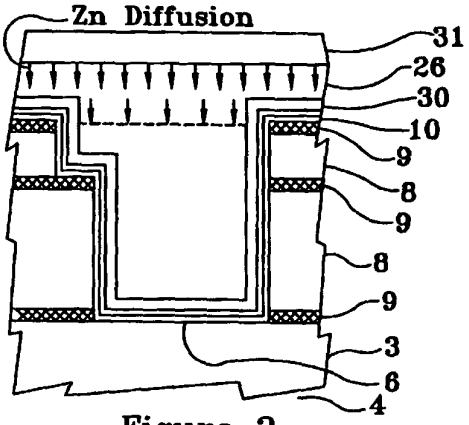


Figure 2

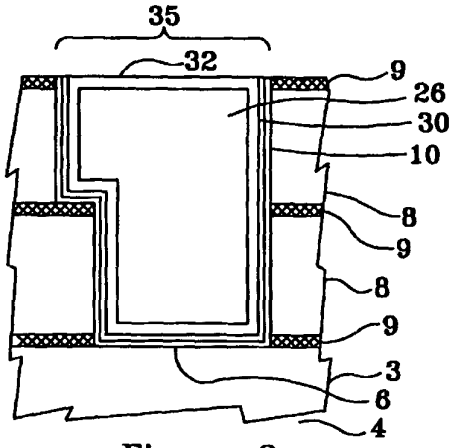


Figure 3

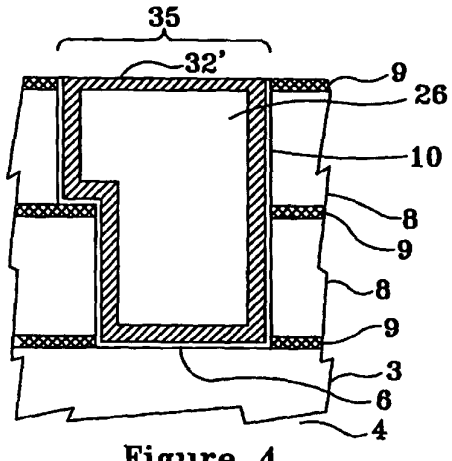


Figure 4

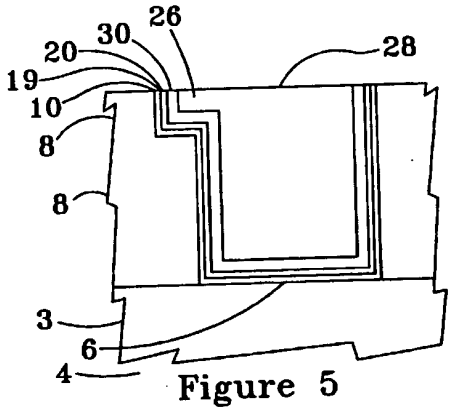


Figure 5

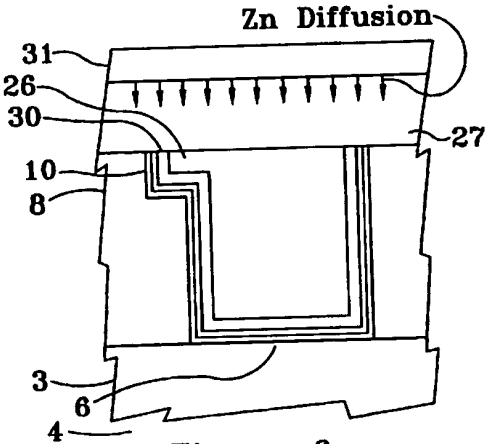


Figure 6

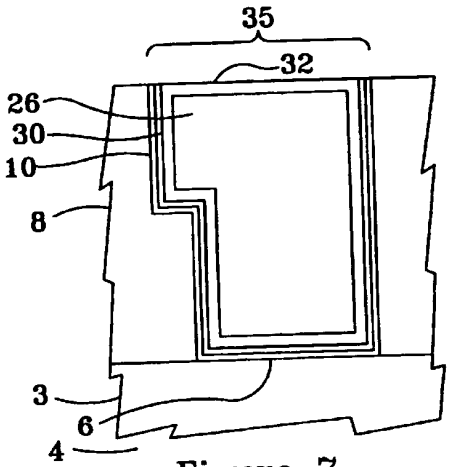


Figure 7

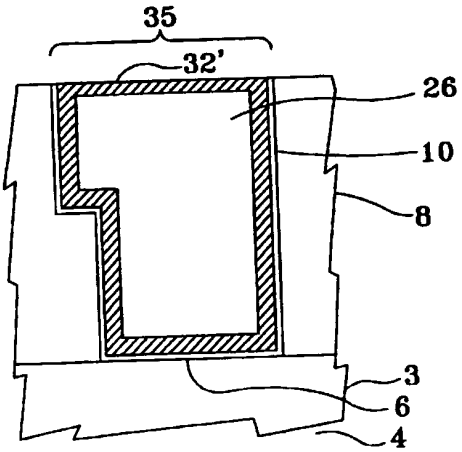
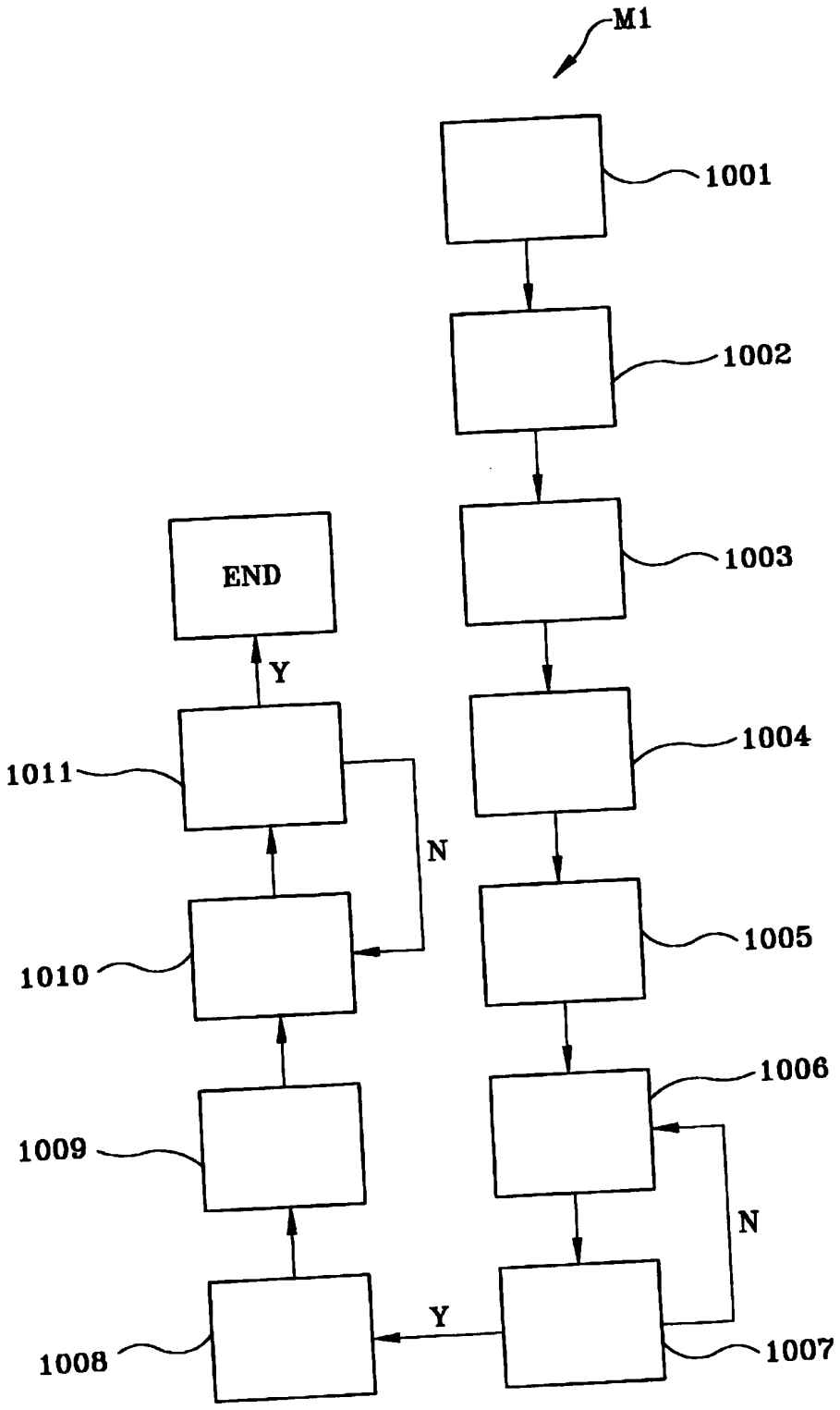


Figure 8


M1
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END
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Figure 9

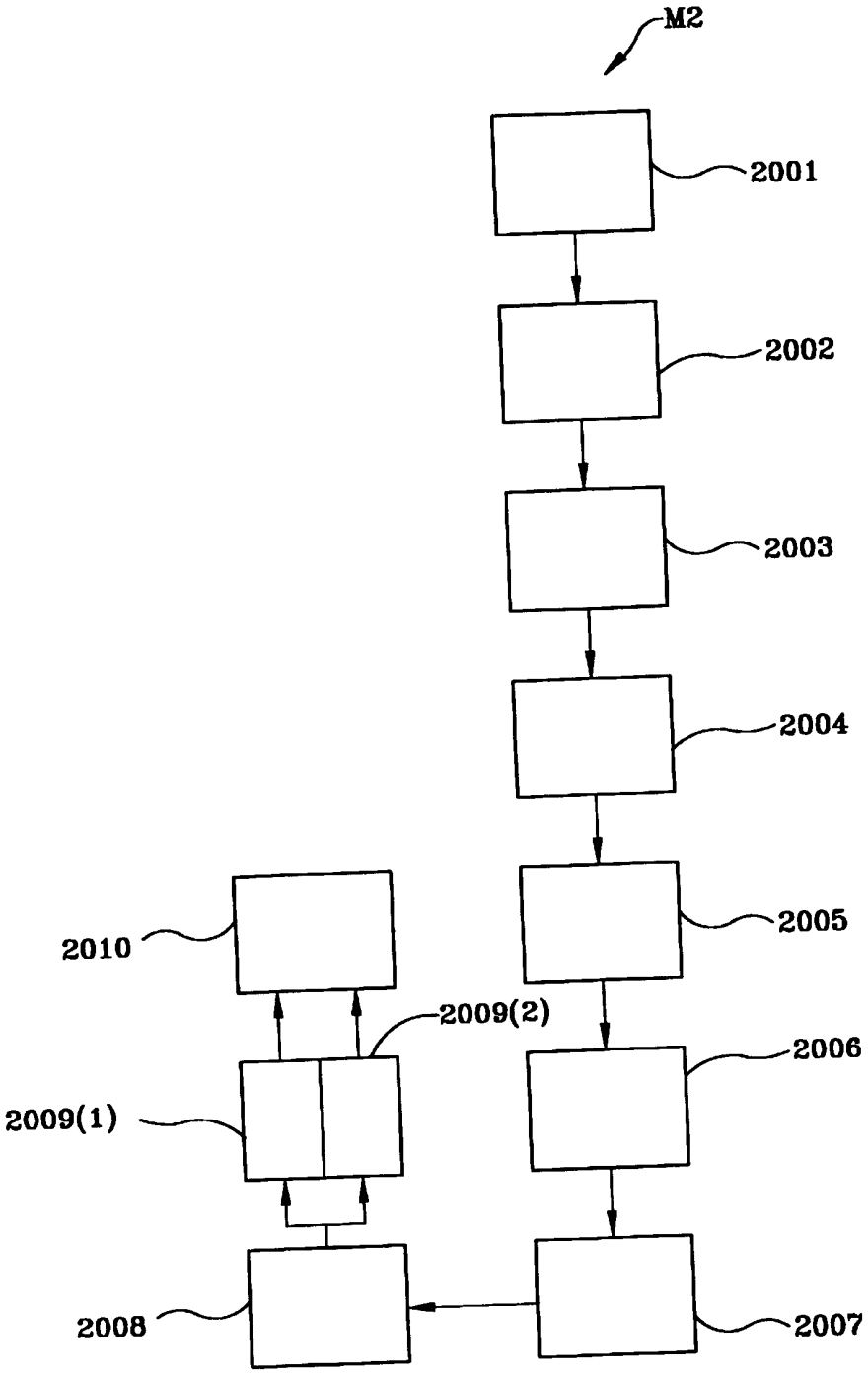

Figure 10

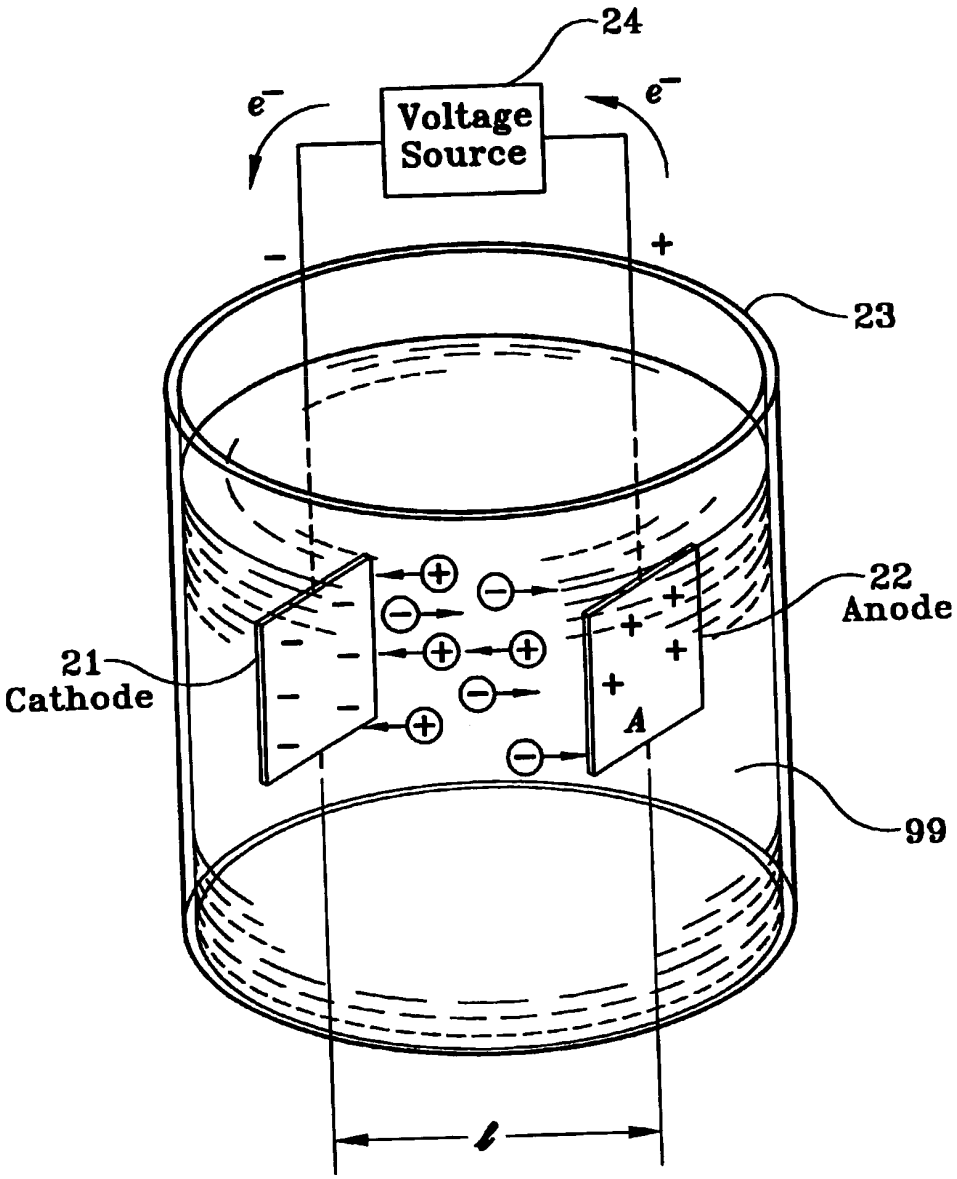

Figure 11

SEMICONDUCTOR DEVICE WITH COPPER-FILLED VIA INCLUDES A COPPER-ZINC/ALLOY FILM FOR REDUCED ELECTROMIGRATION OF COPPER

CROSS-REFERENCE TO RELATED APPLICATION(S)

This application is also related to the following commonly assigned applications:

(1) U.S. Ser. No. 10/081,074, entitled "Chemical Solution for Electroplating a Copper-Zinc Alloy Thin Film, filed Feb. 21, 2002;"

(2) U.S. Ser. No. 10/082,432, entitled "Method of Electroplating a Copper-Zinc Alloy Thin Film on a Copper Surface Using a Chemical Solution and a Semiconductor Device thereby Formed, filed Feb. 22, 2002;"

(3) U.S. Ser. No. 10/082,433, entitled "Method of Controlling Zinc-Doping in a Copper-Zinc Alloy Thin Film Electroplated on a Copper Surface and a Semiconductor Device thereby Formed, filed Feb. 22, 2002;"

(4) U.S. Ser. No. 10/083,809, entitled "Method of Reducing Electromigration in a Copper Line by Electroplating an Interim Copper-Zinc Alloy Thin Film on a Copper Surface and a Semiconductor Device thereby Formed, filed Feb. 26, 2002;"

(5) U.S. Ser. No. 10/084,563, entitled "Method of Reducing Electromigration by Forming an Electroplated Copper-Zinc Interconnect and a Semiconductor Device thereby Formed, filed Feb. 26, 2002;" and

(6) U.S. Ser. No. 10/016,645, entitled "Method of Reducing Electromigration by Ordering Zinc-Doping in an Electroplated Copper-Zinc Interconnect and a Semiconductor Device thereby Formed, filed Dec. 7, 2001."

FIELD OF THE INVENTION

The present invention relates to semiconductor devices and their methods of fabrication. More particularly, the present invention relates to the processing of copper interconnect material and the resultant device utilizing the same. Even more particularly, the present invention relates to reducing electromigration in copper interconnect lines by doping their surfaces with a barrier material using wet chemical methods.

BACKGROUND OF THE INVENTION

Currently, the semiconductor industry is demanding faster and denser devices (e.g., 0.05 μm to 0.25 μm) which implies an ongoing need for low resistance metallization. Such need has sparked research into resistance reduction through the use of barrier metals, stacks, and refractory metals. Despite aluminum's (Al) adequate resistance, other Al properties render it less desirable as a candidate for these higher density devices, especially with respect to its deposition into plug regions having a high aspect ratio cross-sectional area. Thus, research into the use of copper as an interconnect material has been revisited, copper being advantageous as a superior electrical conductor, providing better wettability, providing adequate electromigration resistance, and permitting lower depositional temperatures. The copper (Cu) interconnect material may be deposited by chemical vapor deposition (CVD), plasma-enhanced chemical vapor deposition (PECVD), sputtering, electroless plating, and electrolytic plating.

However, some disadvantages of using Cu as an interconnect material include etching problems, corrosion, and diffusion into silicon.[1] These problems have instigated further research into the formulation of barrier materials for preventing electromigration in both Al and Cu interconnect lines. In response to electromigration concerns relating to the fabrication of semiconductor devices particularly having aluminum-copper alloy interconnect lines, the industry has been investigating the use of various barrier materials such as titanium-tungsten (TiW) and titanium nitride (TiN) layers as well as refractory metals such as titanum (Ti), tungsten (W), tantalum (Ta), molybdenum (Mo), and their silicides.[2] Although the foregoing materials are adequate for Al interconnects and Al—Cu alloy interconnects, they have not been entirely effective

[1]Peter Van Zant, Microchip Fabrication: A Practical Guide to Semiconductor Processing, 3rd Ed., p. 397 (1997).

[2]Id., at 392. with respect to all-Cu interconnects. Further, though CVD and PECVD have been conventionally used for depositing secondary metal(s) on a primary metal interconnect surface, neither technique provides a cost-effective method of forming a copper-zinc alloy on a Cu interconnect surface. Therefore, a need exists for a low cost and high throughput method of reducing electromigration in copper interconnect lines by restricting Cu-diffusion pathways along a Cu surface via doping the Cu surface with Zn from an interim copper-zinc (Cu—Zn) alloy thin film electroplated on the copper (Cu) surface from a stable chemical solution, and controlling the Zn-doping thereof, which also improves interconnect reliability and corrosion resistance.

BRIEF SUMMARY OF THE INVENTION

Accordingly, the present invention provides a method of reducing electromigration in copper interconnect lines by restricting Cu-diffusion pathways along a Cu surface via doping the Cu surface with Zn from an interim copper-zinc (Cu—Zn) alloy thin film electroplated on the copper (Cu) surface from a stable chemical solution, and controlling the Zn-doping thereof, which also improves interconnect reliability and corrosion resistance, and a semiconductor device thereby formed. The present method involves electroplating by immersing the Cu surface, such as a blanket Cu seed layer and a partial thickness plated Cu layer, into a unique nontoxic aqueous chemical electroplating solution containing salts of zinc (Zn) and copper (Cu), their complexing agents, a pH adjuster, and surfactants, thereby forming an interim Cu—Zn alloy thin film having some degree of oxygen (O) concentration, wherein the Zn-doping is controllable by varying the electroplating conditions; and annealing the interim Cu—Zn alloy thin film formed on the Cu surface in an environment such as vacuum, nitrogen (N_2), hydrogen (H_2), formine (N_2H_2), or mixtures thereof for reducing the O-concentration in the alloy thin film layer, for modifying the grain structure of the Cu—Zn alloy thin film as well as of the underlying Cu surface, and for forming a mixed Cu—Zn/Cu interface; and further electroplating the alloy thin film layer with Cu for completely filling the via, thereby forming the interconnect structure. The present invention further provides a particular electroplating method which controls the parameters of Zn concentration, pH, temperature, and time in order to form a uniform reduced-oxygen copper-zinc alloy (Cu—Zn) thin film on a cathode-wafer surface such as a copper (Cu) surface for reducing electromigration in the device by decreasing the drift velocity therein which decreases the Cu migration rate in addition to decreasing the void formation rate.

More specifically, the present invention provides a method of fabricating a semiconductor device, having a first interim reduced-oxygen copper-zinc alloy (Cu—Zn) thin film formed on a copper (Cu) surface and a second interim reduced-oxygen Cu—Zn alloy thin film formed on a Cu-fill, both films being formed by electroplating the Cu surface and the Cu-fill, respectively, in a chemical solution, generally comprising the steps of: providing a semiconductor substrate

having a Cu surface, an optional barrier layer, and an optional underlayer formed in a via; providing a chemical solution; immersing the Cu surface in the chemical solution, thereby forming a first interim Cu—Zn alloy thin film on the Cu surface; rinsing the first interim Cu—Zn alloy thin film in a solvent; drying the first interim Cu—Zn alloy thin film under a gaseous flow; annealing the first interim Cu—Zn alloy thin film formed on the Cu surface, thereby forming a first interim reduced-oxygen Cu—Zn alloy thin film; filling the via with Cu on the first interim reduced-oxygen Cu—Zn alloy thin film, thereby forming a Cu-fill; annealing the Cu-fill, the first interim reduced-oxygen Cu—Zn alloy thin film, the Cu surface, the optional barrier layer, and the optional underlayer; immersing the annealed Cu-fill in the chemical solution, thereby forming a second interim Cu—Zn alloy thin film on the annealed Cu-fill; rinsing the second interim Cu—Zn alloy thin film in a solvent; drying the second interim Cu—Zn alloy thin film under a gaseous flow, for instance, under a gaseous nitrogen flow (GN_2); annealing second interim Cu—Zn alloy thin film formed on the Cu-fill, thereby diffusing a plurality of Zn ions from the second interim Cu—Zn alloy thin film into the Cu-fill, and thereby forming a second interim reduced-oxygen Cu—Zn alloy thin film comprising the second interim Cu—Zn alloy thin film as well as an upper portion of the Cu-fill; planarizing second interim reduced-oxygen Cu—Zn alloy thin film, the Cu-fill, the first interim reduced-oxygen Cu—Zn alloy thin film, the Cu surface, the optional barrier layer, and the optional underlayer, thereby forming an encapsulated dual-inlaid interconnect structure; and completing formation of the semiconductor device.

By electroplating this Cu—Zn alloy thin film on the cathode-wafer surface such as a Cu surface using a stable chemical solution in the prescribed concentration ranges and by subsequently annealing the Cu—Zn alloy thin film electroplated on the Cu surface, the present invention improves Cu interconnect reliability, enhances electromigration resistance, improves corrosion resistance, and reduces manufacturing costs. In particular, the present invention chemical solution is advantageous in that it facilitates formation of an acceptable Cu—Zn alloy thin film over a wide range of bath compositions while the subsequent annealing step removes undesirable oxygen impurities from the formed alloy thin film. The desirable Zn concentration in the Cu—Zn alloy thin film, preferably in a range of approximately 0.2 at. % to approximately 9.0 at. % determined by X-Ray Photoelectron Spectroscopy (XPS) or Auger Electron Spectroscopy (AES), is controllable by varying the electroplating conditions and/or the bath composition. By so controlling the Zn-doping, the present method balances high electromigration performance against low resistivity requirements. Additionally, the Cu surface (e.g., seed layer), being formed by a technique such as electroless deposition, ion metal plasma (IMP), self-ionized plasma (SIP), hollow cathode magnetron (HCM), chemical vapor deposition (CVD), and atomic layer deposition (ALD), is enhanced by the Cu—Zn alloy thin film and is prevented from etching by the high pH value (i.e., basic) of the chemical solution from which the alloy thin film is formed.

Further advantages arise from the present invention's superior fill-characteristics. The present Cu—Zn electroplating solution facilitates better filling of a Cu—Zn alloy thin film on an interconnect, especially for feature sizes in a dimensional range of approximately 0.2 μm to approximately 0.05 μm, thereby lowering the resistance of the formed Cu—Zn alloy thin film (e.g., in a resistance range of approximately 2.2 $\mu\Omega$·cm to approximately 2.5 $\mu\Omega$·cm for approximately 1 at. % Zn content in a Cu—Zn alloy thin film, as deposited). Further, the filling capability is enhanced by three beneficial characteristics of the present invention: (1) the instant chemical solution does not etch copper or a copper alloy seed layer; (2) the introduction of Zn into the alloy thin film as well as onto the Cu interconnect improves both step coverage and nucleation; and (3) a variety of organic additives, such as polyethylene glycol (PEG), organo-disulfides, and organo-chlorides, are compatible and maybe included in the instant chemical solution for further enhancing the fill profile and grain structure. The present Cu—Zn electroplating solution provides a desirably low Zn content in a Cu alloy interconnect (e.g., in a concentration range of approximately 0.2 at. % to approximately 1.0 at. %) which also imparts (1) a de minimis increase in resistance as well as (2) a maximum improvement in electromigration resistance. The present chemical solution can also provide a desirably low Zn content (e.g., in a range of <<approximately 0.1 at. % or <<approximately 0.2 at. %, virtually undetectable by AES) in a Cu film, wherein the Zn content may be engineered by varying the deposition parameters as well as by modifying the bath composition.

BRIEF DESCRIPTION OF THE DRAWING(S)

For a better understanding of the present invention, reference is made to the below-referenced accompanying drawings. Reference numbers refer to the same or equivalent parts of the present invention throughout the several figures of the drawings.

(1) FIG. **1** is a cross-sectional view of a Cu interconnect line formed on a semiconductor substrate and acting as the bottom portion of a via, the via sidewalls comprising at least one low dielectric constant layer and at least one high dielectric constant step layer, the via having an optional barrier layer formed therein, an optional underlayer formed on the optional barrier layer, and a Cu surface (e.g., a seed layer) formed on the optional underlayer, a first interim Cu—Zn alloy thin film formed and annealed on the Cu surface, and a Cu-fill formed on the first interim Cu—Zn alloy thin film, in accordance with a first embodiment of the present invention.

(2) FIG. **2** is a cross-sectional view of the features as shown in FIG. **1**, further having a second interim Cu—Zn alloy thin film formed and annealed on the Cu-fill, having Zn diffusion down (Zn-doping) into an upper portion of the Cu-fill, in accordance with the first embodiment of the present invention.

(3) FIG. **3** is a cross-sectional view of the features as shown in FIG. **2**, further having been planarized which forms an encapsulated dual-inlaid interconnect structure, in accordance with the first embodiment of the present invention.

(4) FIG. **4** is a cross-sectional view of the features of FIG. **3**, wherein the encapsulated dual-inlaid interconnect structure comprises a mixed layer, and wherein the mixed layer comprises the annealed and planarized second interim Cu—Zn alloy thin film and the first interim Cu—Zn alloy thin film , and the Cu-fill, in accordance with the first embodiment of the present invention.

(5) FIG. **5** is a cross-sectional view of a Cu interconnect line formed on a semiconductor substrate and acting as the bottom portion of a via, the via sidewalls comprising at least one low dielectric constant layer, the via having an optional barrier layer formed therein, an optional underlayer formed on the optional barrier layer, and a Cu surface (e.g., a seed layer) formed on the optional underlayer, a first interim

Cu—Zn alloy thin film formed and annealed on the Cu surface, and a Cu-fill formed first interim Cu—Zn alloy thin film, the first interim Cu—Zn alloy thin film, the Cu-fill, the Cu surface, the optional underlayer, and the optional barrier layer having been planarized to form an intermediate planarized surface, in accordance with a second embodiment of the present invention.

(6) FIG. **6** is a cross-sectional view of the features as shown in FIG. **5**, further having a Cu layer deposited on the intermediate planarized surface a second interim Cu—Zn alloy thin film formed and annealed on the Cu layer, and having Zn diffusion down (Zn-doping) through the Cu layer and into an upper portion of the Cu-fill, in accordance with the second embodiment of the present invention.

(7) FIG. **7** is a cross-sectional view of Figure the features as shown in **6**, having been further planarized which forms an encapsulated dual-inlaid interconnect structure, in accordance with the second embodiment of the present invention.

(8) FIG. **8** is a cross-sectional view of the features of FIG. **7**, wherein the encapsulated dual-inlaid interconnect structure comprises a mixed layer, and wherein the mixed layer comprises the annealed and planarized second interim Cu—Zn alloy thin film and the first interim Cu—Zn alloy thin film, and the Cu-fill, in accordance with the second embodiment of the present invention.

(9) FIG. **9** is a flowchart of a method for synthesizing a unique nontoxic aqueous Cu—Zn electroplating (chemical) solution, in accordance with the present invention.

(10) FIG. **10** is a flowchart of a method for forming a Cu—Zn alloy thin film on a Cu surface, in accordance with the present invention.

(11) FIG. **11** is a perspective view of an electroplating apparatus using the unique nontoxic aqueous Cu—Zn chemical solution, in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

FIG. **1** illustrates, by example only, a cross-section of a Cu interconnect line **3** formed on a semiconductor substrate **4** and acting as the bottom portion of a via **6**, the via **6** sidewalls comprising at least one low dielectric constant layer **8** and at least one high dielectric constant step layer **9**, the via **6** having an optional barrier layer **10** formed therein, an optional underlayer **19** formed on the optional barrier layer **10**, and a Cu surface (e.g., a seed layer) **20** in a thickness range of approximately 100 Å to approximately 300 Å formed on the optional underlayer **19**, a first interim Cu—Zn alloy thin film **30** formed and annealed on the Cu surface **20**, and a Cu-fill **26** formed on the first interim Cu—Zn alloy thin film **30**, in accordance with a first embodiment of the present invention. The optional barrier layer **10** comprises at least one material selected from a group consisting essentially of titanium silicon nitride ($Ti_xSi_yN_z$) tantalum nitride (TaN), and tungsten nitride (W_x, N_y) has a thickness range of approximately 10 Å to approximately 30 Å and is formed by a technique such as atomic layer deposition (ALD), atomic layer chemical vapor deposition (ALCVD), or chemical vapor deposition (CVD). The optional underlayer **19** comprises at least one material selected from a group consisting essentially of tin (Sn) and Palladium (Pd) in a thickness range of approximately 10 Å approximately 30 Å.

FIG. **2** illustrates, in cross-section, the features of FIG. **1**, further having a second interim Cu—Zn alloy thin film **31** formed and annealed on the Cu-fill **26**, having Zn diffusion down (Zn-doping) into an upper portion of the Cu-fill, **26** in accordance with the first embodiment of the present invention. The optional underlayer **19** is not shown.

FIG. **3** illustrates, in cross-section, the features of FIG. **2**, further having been planarized which forms an annealed and planarized second interim Cu—Zn alloy thin film **32** and an encapsulated dual-inlaid interconnect structure **35**, in accordance with the first embodiment of the present invention. The optional underlayer **19** is not shown.

FIG. **4** illustrates, in cross-section, the features of FIG. **3**, wherein the encapsulated dual-inlaid interconnect structure **35** comprises a mixed layer **32'** and the Cu-fill **26**, wherein the mixed layer **32'** comprises the annealed and planarized second interim Cu—Zn alloy thin film **32** and the first interim Cu—Zn alloy thin film **30**, in accordance with the first embodiment of the present invention. The encapsulated dual-inlaid interconnect structure **35** may also comprise the optional barrier layer **10** and the optional underlayer **19** (not shown).

FIG. **5** illustrates, by example only, a cross-section of a Cu interconnect line **3** formed on a semiconductor substrate **4** and acting as the bottom portion of a via **6**, the via **6** sidewalls comprising at least one low dielectric constant layer **8**, the via **6** having an optional barrier layer **10** formed therein, an optional underlayer **19** formed on the optional barrier layer **10**, and a Cu surface (e.g., a seed layer) **20** in a thickness range of approximately 100 Å to approximately 300 Å formed on the optional underlayer **19**, a first interim Cu—Zn alloy thin film **30** formed and annealed on the Cu surface **20**, and a Cu-fill **26** formed on the first interim Cu—Zn alloy thin film **30**, the first interim Cu—Zn alloy thin film **30**, the Cu-fill **26**, the Cu surface **20**, the optional underlayer **19**, and the optional barrier layer **10** having been planarized to form an intermediate planarized surface **28**, in accordance with a second embodiment of the present invention. The optional barrier layer **10**, comprising at least one material selected from a group consisting essentially of titanium silicon nitride ($Ti_xSi_yN_z$), tantalum nitride (TaN), and tungsten nitride (W_xN_y) has a thickness range of approximately 10 Å to approximately 30 Å and is formed by a technique such as atomic layer deposition (ALD), atomic layer chemical vapor deposition (ALCVD), or chemical vapor deposition (CVD). The optional underlayer **19** comprises at least one material selected from a group consisting essentially of tin (Sn) and Palladium (Pd) in a thickness range of approximately 10 Å to approximately 30 Å.

FIG. **6** illustrates, in cross-section, the features of FIG. **5**, further having a Cu layer **27** deposited on the intermediate planarized surface **28**, a second interim Cu—Zn alloy thin film **31** formed and annealed on the Cu layer **27**, and having Zn diffusion down (Zn-doping) through the Cu layer **27** and into an upper portion of the Cu-fill **26**, in accordance with the second embodiment of the present invention.

FIG. **7** illustrates, in cross-section, the features of FIG. **6**, having been further planarized which forms an annealed second interim Cu—Zn alloy thin film **32** and an encapsulated dual-inlaid interconnect structure **35**, in accordance with the second embodiment of the present invention.

FIG. **8** illustrates, in cross-section, the features of FIG. **7**, wherein the encapsulated dual-inlaid interconnect structure **35** comprises a mixed layer **32'** and the Cu-fill **26**, wherein the mixed layer **32'** comprises the annealed and planarized second interim Cu—Zn alloy thin film **32** and the first interim Cu—Zn alloy thin film **30**, in accordance with the second embodiment of the present invention. The encapsulated dual-inlaid interconnect structure **35** may also comprise the optional barrier layer **10** and the optional underlayer **19** (not shown).

FIG. **9** flowcharts, by example only, a method M1 for synthesizing a liter of a unique nontoxic aqueous Cu—Zn electroplating (chemical) solution, in accordance with the present invention:

(1) cleaning a mixing vessel (e.g., a beaker) with dilute nitric acid (HNO_3) for approximately 5 minutes, as indicated by block **1001**;

(2) rinsing the mixing vessel in deionized (DI) water for approximately 5 minutes to approximately 10 minutes and subsequently drying the mixing vessel, for instance, under a gaseous nitrogen (GN_2) flow, as indicated by block **1002**;

(3) adding an initial volume of DI water (e.g., approximately 400 ml) to the mixing vessel, as indicated by block **1003**;

(4) adding at least one Cu ion source for providing a plurality of Cu ions and stirring the at least one Cu ion source into the DI water for a duration in a range of approximately 5 minutes to approximately 10 minutes or until complete dissolution of the at least one Cu ion source in the DI water is achieved, as indicated by block **1004**;

(5) adding at least one complexing agent for complexing the plurality of Cu ions and stirring the at least one complexing agent until complete dissolution of the at least one complexing agent in the DI water is achieved, as indicated by block **1005**;

(6) adding at least one pH adjuster and stirring the at least one pH adjuster into the DI water for a duration in a range of approximately 5 minutes to approximately 10 minutes or until a clean and transparent solution is achieved, as indicated by block **1006**;

(7) measuring the pH of the solution, and, if the pH is within the desired range, proceeding to step (8), otherwise titrating the solution with a small volume of the at least one pH adjuster until the pH falls within the desired range, in essence, returning to step (6), as indicated by block **1007**;

(8) adding at least one Zn ion source for providing a plurality of Zn ions and stirring the at least one Zn ion source into the DI water for a duration in a range of approximately 5 minutes to approximately 10 minutes or until complete dissolution of the at least one Zn ion source in the DI water is achieved, as indicated by block **1008**;

(9) adding a final volume of DI water (e.g., effecting approximately 1 L in total solution volume) to the mixing vessel, as indicated by block **1009**;

(10) optionally adding at least one complexing agent for complexing the plurality of Zn ions and stirring the at least one complexing agent until complete dissolution of the at least one complexing agent in the DI water is achieved, as indicated by block **1010**; and

(11) measuring the pH of the solution, and, if the pH is within the desired range, terminating the synthesis, otherwise further titrating the solution with a small volume of the at least one pH adjuster until the pH falls within the desired range, in essence, returning to step (10), as indicated by block **1011**.

In addition, the present invention chemical solution may be formulated as follows: wherein the at least one zinc (Zn) ion source comprises at least one zinc salt selected from a group consisting essentially of zinc acetate ($(CH_3CO_2)_2Zn$), zinc bromide ($ZnBr_2$), zinc carbonate hydroxide ($ZnCO_3{\cdot}2Zn(OH)_2$), zinc dichloride ($ZnCl_2$), zinc citrate ($(O_2CCH_2C(OH)(CO_2)CH_2CO_2)_2Zn_3$), zinc iodide ($ZnI_2$), zinc L-lactate ($(CH_3CH(OH)CO_2)_2Zn$), zinc nitrate ($Zn(NO_3)_2$), zinc stearate ($(CH_3(CH_2)_{16}CO_2)_2Zn$), zinc sulfate ($ZnSO_4$), zinc sulfide (ZnS), zinc sulfite ($ZnSO_3$), and their hydrates (preferably zinc chloride or zinc dichloride and zinc citrate), wherein the at least one complexing agent for complexing the plurality of Zn ions comprises tartaric acid ($HO_2CCH(OH)CH(OH)CO_2H$), wherein the tartaric acid prevents precipitation of the plurality of Zn ions from the chemical solution, wherein the at least one copper (Cu) ion source comprises at least one copper salt selected from a group consisting essentially of copper(I) acetate (CH_3CO_2Cu), copper(II) acetate ($(CH_3CO_2)_2Cu$), copper(I) bromide (CuBr), copper(II) bromide ($CuBr_2$), copper(II) hydroxide ($Cu(OH)_2$), copper(II) hydroxide phosphate ($Cu_2(OH)PO_4$), copper(I) iodide (CuI), copper(II) nitrate ($(CuNO_3)_2$), copper(II) sulfate ($CuSO_4$), copper(I) sulfide (Cu_2S), copper(II) sulfide (CuS), copper(II) tartrate ($(CH(OH)CO_2)_2Cu$), and their hydrates (preferably copper sulfate), wherein the at least one complexing agent for the plurality of Cu ions comprises at least one species selected from a group consisting essentially of ethylene diamine "EDA" ($H_2NCH_2CH_2NH_2$) and ethylenediaminetetraacetic acid "EDTA" ($(HO_2CCH_2)_2NCH_2CH_2N(CH_2CO_2H)_2$), wherein the EDTA prevents precipitation of the plurality of Cu ions from the chemical solution, wherein the at least one pH adjuster comprises at least one pH-adjusting compound selected from a group of pH-adjusting compounds consisting essentially of ammonium hydroxide (NH_4OH) and tetramethylammonium hydroxide "TMAH" ($(CH_3)_4NOH$), wherein the at least one wetting agent comprises a surfactant, and wherein the surfactant comprises at least one surfactant selected from a group consisting essentially of RE-610™ and polyethylene glycol (PEG).

In the preferred embodiment of the chemical solution, the composition of the method M1 is formulated with component concentration ranges as follows: wherein the at least one zinc (Zn) ion source is provided in a concentration range of approximately 5 g/L to approximately 10 g/L (preferably approximately 10 g/L), wherein the at least one complexing agent for complexing the plurality of Zn ions is provided in a concentration range of approximately 10 g/L to approximately 30 g/L (preferably approximately 20 g/L), wherein the at least one copper (Cu) ion source is provided in a concentration range of approximately 5 g/L to approximately 20 g/L (preferably approximately 10 g/L), wherein the at least one complexing agent for complexing the plurality of Cu ions is provided in a concentration range of approximately 40 g/L to approximately 100 g/L (preferably approximately 80 g/L), wherein the at least one pH adjuster is provided in a concentration range of approximately 10 g/L to approximately 20 g/L (preferably approximately 15 g/L), wherein the at least one wetting agent is provided in a concentration range of approximately 0.01 g/L to approximately 0.1 g/L (preferably approximately 0.02 g/L), wherein the volume of water is provided in a volume range of up to and including approximately 1 L, wherein the solution flow rate is in a range of approximately less than 3 L/min, wherein the solution stir rate is in a range of approximately less than 700 rpm, and wherein the wafer rotation rate is in a range of approximately less than or equal to 700 rpm.

Also, the preferred embodiment involves the following process parameters ranges: wherein the at least one pH adjuster adjusts the chemical solution to a pH range of approximately 7 to approximately 14 (preferably in a pH range of approximately 10 to approximately 12), wherein the chemical solution maybe maintained in a temperature

range of approximately 16° C. to approximately 35° C. (preferably at a temperature of approximately 24° C.), wherein the Cu surface **20** is immersed for a duration in a range of approximately 30 seconds to approximately 120 seconds (preferably for a duration of approximately 60 sec), wherein the Cu—Zn alloy thin film **30** is formed having a thickness in a range of approximately 10 nm (100 Å) to approximately 200 nm (2 Å) (preferably having a thickness of approximately 30 nm), and wherein the formed Cu-rich Cu—Zn alloy thin film **30** has a low Zn content of approximately 10 at. % and a high Cu content of approximately 90 at. % (preferably~1–2 at. % Zn :~98–99 at. % Cu).

FIG. **10** flowcharts, by example only, a method M2 of fabricating a semiconductor device, having a first interim reduced-oxygen copper-zinc (Cu—Zn) alloy thin film **30** formed on a copper (Cu) surface **20**, the Cu surface **20** having been formed by CVD, PVD, PECVD or electroplating, and a second interim reduced-oxygen Cu—Zn alloy thin film **31** formed on either a Cu-fill **26** or a Cu layer **27**, both films **30**, **31** being formed by electroplating the Cu surface **20** and either the Cu-fill **26** or a Cu layer **27**, respectively, in a chemical solution, initially comprising the steps of: providing a semiconductor substrate **4** having a Cu surface **20**, an optional barrier layer **10**, and an optional underlayer **19** formed in a via **6**, as indicated by block **2001**; providing a chemical solution, the chemical solution comprising: at least one zinc (Zn) ion source for providing a plurality of Zn ions; at least one copper (Cu) ion source for providing a plurality of Cu ions; at least one complexing agent for complexing the plurality of Cu ions; at least one pH adjuster; at least one wetting agent for stabilizing the chemical solution, all being dissolved in a volume of deionized (DI) water, as shown by block **2002**; electroplating the Cu surface **20** in the chemical solution, thereby forming a first interim Cu—Zn alloy thin film **30** on the Cu surface **20**, as indicated by block **2003**; rinsing the first interim Cu—Zn alloy thin film **30** in a solvent, as indicated by block **2004**; drying the first interim Cu—Zn alloy thin film **30** under a gaseous flow, for instance, under a gaseous nitrogen flow (GN_2), as indicated by block **2005**; annealing the first interim Cu—Zn alloy thin film **30** formed on the Cu surface **20** in a temperature range such as 150° C. to 450° C. (preferably in a temperature of approximately 150° C. to approximately 250° C.), wherein the annealing step is performed for a duration range of approximately 0.5 minutes to approximately 60 minutes, thereby reducing the oxygen impurity concentration to a level less than that which is detectable (i.e.,~0.1 at. %) in the alloy thin film **30**, thereby modifying the grain structure by increasing the grain size of both the alloy thin film **30** as well as the Cu surface **20**, and thereby forming a first interim reduced-oxygen Cu—Zn alloy thin film **30**, as indicated by block **2006**; filling the via **6** with Cu on the first interim reduced-oxygen Cu—Zn alloy thin film **30**, thereby forming a Cu-fill **26**, as indicated by block **2007**; and annealing the Cu-fill **26**, the first interim reduced-oxygen Cu—Zn alloy thin film **30**, the Cu surface **20**, the optional barrier layer **10**, and the optional underlayer **19**, the underlayer **19** comprising at least one material selected from a group consisting essentially of tin (Sn) and palladium (Pd), as indicated by block **2008**. The chemical solution may also further comprises at least one complexing agent for complexing the plurality of Zn ions also being dissolved in the volume of DI water.

The method M2 subsequently comprises the steps of: subjecting the annealed Cu-fill **26**, the first interim reduced-oxygen Cu—Zn alloy thin film **30**, the Cu surface **20**, the optional barrier layer **10**, and the optional underlayer **19** to a process selected from a group consisting essentially of: process (1) comprising the steps of: immersing the annealed Cu-fill **26** in the chemical solution, thereby forming a second interim Cu—Zn alloy thin film **31** on the annealed Cu-fill **26**; rinsing the second interim Cu—Zn alloy thin film **31** in a solvent; drying the second interim Cu—Zn alloy thin film **31** under a gaseous flow, for instance, under a gaseous nitrogen flow (GN_2); annealing the second interim Cu—Zn alloy thin film layer **31** formed on the Cu-fill **26** in a temperature range such as 150° C. to 450° C. (preferably in a temperature of approximately 150° C. to approximately 250° C.), wherein the annealing step is performed for a duration range of approximately 0.5 minutes to approximately 60 minutes, thereby reducing the oxygen impurity concentration to a level less than that which is detectable (i.e.,~0.1 at. %) in the second interim Cu—Zn alloy thin film layer **31**, thereby modifying the grain structure by increasing the grain size of both the second interim Cu—Zn alloy thin film layer **31** as well as the Cu fill **26**, and thereby forming a reduced-oxygen mixed Cu—Zn interface **25'**, thereby diffusing a plurality of Zn ions from the second interim Cu—Zn alloy thin film **31** into the Cu-fill **26**, and thereby forming a second interim reduced-oxygen Cu—Zn alloy thin film **32** comprising the second interim Cu—Zn alloy thin film **31** as well as an upper portion of the Cu-fill **26**; and planarizing, by a technique such as chemical mechanical polishing (CMP), the second interim reduced-oxygen Cu—Zn alloy thin film **32**, the Cu-fill **26**, the first interim reduced-oxygen Cu—Zn alloy thin film **30**, the Cu surface **20**, the optional barrier layer **10**, and the optional underlayer **19**, thereby completing formation of an encapsulated dual-inlaid interconnect structure **35**, as indicated by block **2009**(1); and process (2) comprising the steps of: planarizing the Cu-fill **26**, the first interim reduced-oxygen Cu—Zn alloy thin film **30**, the Cu surface **20**, the optional barrier layer **10**, and the optional underlayer **19**, thereby forming an intermediate planarized surface **28**; depositing a Cu layer **27**, in a thickness range of approximately 3 nm to approximately 50 nm, on the intermediate planarized surface **28**; immersing the Cu layer **27** in the chemical solution, thereby forming a second interim Cu—Zn alloy thin film **31** on the Cu layer **27**; rinsing the second interim Cu—Zn alloy thin film **31** in a solvent; drying the second interim Cu—Zn alloy thin film **31** under a gaseous flow, for instance, under a gaseous nitrogen flow (GN_2); annealing the second interim Cu—Zn alloy thin film **31** formed on the Cu layer **27**, thereby diffusing a plurality of Zn ions from the second interim Cu—Zn alloy thin film **31** through the Cu layer **27** and into the Cu-fill **26**, and thereby forming a second interim reduced-oxygen Cu—Zn alloy thin film **32** comprising the second interim Cu—Zn alloy thin film **31**, the Cu layer **27**, and an upper portion of the Cu-fill **26**; and planarizing, by a technique such as chemical mechanical polishing (CMP), the annealed second interim reduced-oxygen Cu—Zn alloy thin film **32**, the Cu layer **27**, the Cu-fill **26**, the first interim reduced-oxygen Cu—Zn alloy thin film **30**, the Cu surface **20**, the optional barrier layer **10**, and the optional underlayer **19**, thereby completing formation of an encapsulated dual-inlaid interconnect structure **35**, as indicated by block **2009**(2); and completing formation of the semiconductor device, as indicated by block **2010**. In the second embodiment of the present invention, the annealing step also facilitates doping of the interim Cu—Zn alloy thin film layer **30** with desirable Sn and Pd impurities from the underlayer **19** which structurally stabilizes the film layer **30** by internally increasing its bond strengths.

FIG. **11** illustrates, in perspective view, an electroplating apparatus using the unique nontoxic aqueous Cu—Zn

chemical solution, in accordance with the present invention. In particular, the electroplating step (3) of FIG. **3** step, as indicated by block **2003** in FIG. **10**, may be performed in this electroplating apparatus comprising: (a) a cathode-wafer **21**; (b) an anode **22**; (c) an electroplating vessel **23** such as a beaker; and (d) a voltage source **24**. The cathode-wafer **21** may comprise a Cu surface **20**. The anode **22** may comprise at least one material selected from a group consisting essentially of copper (Cu), a copper-platinum alloy (Cu—Pt), titanium (Ti), platinum (Pt), a titanium-platinum alloy (Ti—Pt), anodized copper-zinc alloy (Cu—Zn, i.e., brass), and platinized titanium (Pt/Ti), and platinized copper-zinc (Pt/Cu—Zn, i.e., platinized brass). The brass alloy may be anodized to form a thin oxide film in situ using the chemical solution **99** prior to electroplating the cathode-wafer **21**. The anodized brass anode also provides the following benefits: (1) a uniform current density distribution on the cathode-wafer; (2) a uniform Cu—Zn alloy thin film formation, (3) a uniform Zn distribution across the Cu—Zn alloy thin film surface, and (4) a uniform Zn distribution across the Cu—Zn alloy thin film thickness. The present invention electroplating method also comprises direct voltage in the range of approximately 1 V to approximately 4 V (preferably in a voltage range of approximately 1 V to approximately 2 V); and a direct current in the range of approximately 0.01 A to approximately 0.2 A (preferably in a current range of approximately 0.1 A to approximately 0.15 A). Differential pulse conditions selected from a group consisting essentially of forward pulses, reverse pulses, combinations of forward and reverse pulses, combinations of direct current, and combinations of direct voltage may also be applied.

Further, the Zn-doping in the resultant Cu—Zn alloy thin film **30** may be controlled in the present invention by varying electroplating conditions. For example, increasing the at least one zinc (Zn) ion source concentration slowly increases Zn-doping, increasing the at least one copper (Cu) ion source concentration slowly decreases Zn-doping, increasing the solution flow rate increases Zn-doping, increasing the pH decreases cathodic efficiency with respect to Zn and thereby decreases Zn-doping, increasing the immersing duration slowly decreases Zn-doping, using a Cu anode decreases Zn-doping, using a brass anode increases Zn-doping, increasing the voltage increases the Zn-doping, and increasing the current increases the Zn-doping.

Information as herein shown and described in detail is fully capable of attaining the above-described object of the invention, the presently preferred embodiment of the invention, and is, thus, representative of the subject matter which is broadly contemplated by the present invention. The scope of the present invention fully encompasses other embodiments which may become obvious to those skilled in the art, and is to be limited, accordingly, by nothing other than the appended claims, wherein reference to an element in the singular is not intended to mean "one and only one" unless explicitly so stated, but rather "one or more." All structural and functional equivalents to the elements of the above-described preferred embodiment and additional embodiments that are known to those of ordinary skill in the art are hereby expressly incorporated by reference and are intended to be encompassed by the present claims.

Moreover, no requirement exists for a device or method to address each and every problem sought to be resolved by the present invention, for such to be encompassed by the present claims. Furthermore, no element, component, or method step in the present disclosure is intended to be dedicated to the public regardless of whether the element, component, or method step is explicitly recited in the claims. However, it should be readily apparent to those of ordinary skill in the art that various changes and modifications in form, semiconductor material, and fabrication material detail may be made without departing from the spirit and scope of the inventions as set forth in the appended claims. No claim herein is to be construed under the provisions of 35 U.S.C. §112, sixth paragraph, unless the element is expressly recited using the phrase "means for."

What is claimed:

1. A semiconductor device, having a first interim reduced-oxygen copper-zinc alloy (Cu—Zn) thin film formed on a copper (Cu) surface and a second interim reduced-oxygen Cu—Zn alloy thin film formed on a Cu-fill, both films being formed by electroplating the Cu surface and the Cu-fill, respectively, in a chemical solution, comprising:

a semiconductor substrate having a via; and

an encapsulated dual-inlaid interconnect structure formed and disposed in said via, said interconnect structure comprising:

at least one Cu surface formed in said via;

a first interim reduced-oxygen Cu—Zn alloy thin film formed and disposed on the at least one Cu surface;

a Cu-fill formed and disposed on said first interim reduced-oxygen Cu—Zn alloy thin film; and

a second interim reduced-oxygen Cu—Zn alloy thin film formed and disposed on the Cu-fill.

2. A semiconductor device, having a first interim reduced-oxygen copper-zinc (Cu—Zn) alloy thin film formed on a copper (Cu) surface and a second interim reduced-oxygen Cu—Zn alloy thin film formed on a Cu-fill, both films being formed by electroplating the Cu surface and the Cu-fill, respectively, in a chemical solution, fabricated by a method comprising the steps of:

providing a semiconductor substrate having a Cu surface formed in a via;

providing a chemical solution;

electroplating the Cu surface in the chemical solution, thereby forming a first interim Cu—Zn alloy thin film on the Cu surface;

rinsing the first interim Cu—Zn alloy thin film in a solvent;

drying the first interim Cu—Zn alloy thin film under a gaseous flow;

annealing the first interim Cu—Zn alloy thin film formed on the Cu surface, thereby forming a first interim reduced-oxygen Cu—Zn alloy thin film;

filling the via with Cu on the first interim reduced-oxygen Cu—Zn alloy thin film, thereby forming a Cu-fill;

annealing the Cu-fill, the first interim reduced-oxygen Cu—Zn alloy thin film, and the Cu surface;

subjecting the annealed Cu-fill, the first interim reduced-oxygen Cu—Zn alloy thin film, and the Cu surface to a process selected from a group consisting essentially of:

process (1) comprising the steps of:

electroplating the annealed Cu-fill in the chemical solution, thereby forming a second interim Cu—Zn alloy thin film on the annealed Cu-fill;

rinsing the second interim Cu—Zn alloy thin film in a solvent;

drying the second interim Cu—Zn alloy thin film under a gaseous flow;

annealing second interim Cu—Zn alloy thin film formed on the Cu-fill, thereby diffusing a plurality

of Zn ions from the second interim Cu—Zn alloy thin film into the Cu-fill, and thereby forming a second interim reduced-oxygen Cu—Zn alloy thin film comprising the second interim Cu—Zn alloy thin film as well as an upper portion of the Cu-fill; and

planarizing second interim reduced-oxygen Cu—Zn alloy thin film, the Cu-fill, the first interim reduced-oxygen Cu—Zn alloy thin film, and the Cu surface, thereby forming an encapsulated dual-inlaid interconnect structure; and

process (2) comprising the steps of:

planarizing the Cu-fill, the first interim reduced-oxygen Cu—Zn alloy thin film, and the Cu surface, thereby forming an intermediate planarized surface;

depositing a Cu layer on the intermediate planarized surface;

electroplating the Cu layer in the chemical solution, thereby forming a second interim Cu—Zn alloy thin film on the Cu layer;

rinsing the second interim Cu—Zn alloy thin film in a solvent;

drying the second interim Cu—Zn alloy thin film under a gaseous flow;

annealing second interim Cu—Zn alloy thin film formed on the Cu layer, thereby diffusing a plurality of Zn ions from the second interim Cu—Zn alloy thin film through the Cu layer and into the Cu-fill, and thereby forming a second interim reduced-oxygen Cu—Zn alloy thin film comprising the second interim Cu—Zn alloy thin film, the Cu layer, and an upper portion of the Cu-fill; and

planarizing the annealed second interim reduced-oxygen Cu—Zn alloy thin film, the Cu layer, the Cu-fill, the first interim reduced-oxygen Cu—Zn alloy thin film, and the Cu surface, thereby forming an encapsulated dual-inlaid interconnect structure; and

completing formation of the semiconductor device.

3. A device, as recited in claim **2**,

wherein the chemical solution is nontoxic and aqueous, and

wherein the chemical solution comprises:

at least one zinc (Zn) ion source for providing a plurality of Zn ions;

at least one copper (Cu) ion source for providing a plurality of Cu ions;

at least one complexing agent for complexing the plurality of Cu ions;

at least one pH adjuster;

at least one wetting agent for stabilizing the chemical solution, all being dissolved in a volume of deionized (DI) water.

4. A device, as recited in claim **3**, wherein the at least one zinc (Zn) ion source comprises at least one zinc salt selected from a group consisting essentially of zinc acetate ($(CH_3CO_2)_2Zn$), zinc bromide ($ZnBr_2$), zinc carbonate hydroxide ($ZnCO_3{\cdot}2Zn(OH)_2$), zinc dichloride ($ZnCl_2$), zinc citrate ($(O_2CCH_2C(OH)(CO_2)CH_2CO_2)_2Zn_3$), zinc iodide ($ZnI_2$), zinc L-lactate ($((CH_3CH(OH)CO_2)_2Zn$), zinc nitrate ($Zn(NO_3)_2$), zinc stearate ($((CH_3(CH_2)_{16}CO_2)_2Zn$), zinc sulfate ($ZnSO_4$), zinc sulfide (ZnS), zinc sulfite ($ZnSO_3$), and their hydrates.

5. A device, as recited in claim **3**, wherein the at least one copper (Cu) ion source comprises at least one copper salt selected from a group consisting essentially of copper(I) acetate (CH_3CO_2Cu), copper(II) acetate ($(CH_3CO_2)_2Cu$), copper(I) bromide (CuBr), copper(II) bromide ($CuBr_2$), copper(II) hydroxide ($Cu(OH)_2$), copper(II) hydroxide phosphate ($Cu_2(OH)PO_4$), copper(I) iodide (CuI), copper(II) nitrate ($(CuNO_3)_2$), copper(II) sulfate ($CuSO_4$), copper(I) sulfide (Cu_2S), copper(II) sulfide (CuS), copper(II) tartrate ($(CH(OH)CO_2)_2Cu$), and their hydrates.

6. A device, as recited in claim **2**,

wherein said electroplating step comprises using an electroplating apparatus, and

wherein said electroplating apparatus comprises:

(a) a cathode-wafer;

(b) an anode;

(c) an electroplating vessel; and

(d) a voltage source.

7. A device, as recited in claim **6**,

wherein the cathode-wafer comprises the Cu surface, and

wherein the anode comprises at least one material selected from a group consisting essentially of copper (Cu), a copper-platinum alloy (Cu—Pt), titanium (Ti), platinum (Pt), a titanium-platinum alloy (Ti—Pt), an anodized copper-zinc alloy (Cu—Zn), a platinized titanium (Pt/Ti), and a platinized copper-zinc (Pt/Cu—Zn).

8. A device, as recited in claim **2**,

wherein said semiconductor substrate further comprises a barrier layer formed in the via under said Cu surface, and

wherein the barrier layer comprises at least one material selected from a group consisting essentially of titanium silicon nitride ($Ti_xSi_yN_z$), tantalum nitride (TaN), and tungsten nitride (W_xN_y).

9. A device, as recited in claim **8**,

wherein said semiconductor substrate further comprises an underlayer formed on the barrier layer,

wherein said underlayer comprises at least one material selected from a group consisting essentially of tin (Sn) and palladium (Pd), and

wherein said Cu surface is formed over said barrier layer and on said underlayer.

10. A device, as recited in claim **9**,

wherein said underlayer comprises a thickness range of approximately 10 Å to approximately 30 Å,

wherein said barrier layer comprises a thickness range of approximately 10 Å to approximately 30 Å,

wherein said Cu surface comprises a thickness range of approximately 100 Å to approximately 300 Å, and

wherein said first interim Cu—Zn alloy thin film comprises a thickness range of approximately 100 Å to approximately 2000 Å.

* * * * *

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(54) **METALLIZATION STRUCTURES FOR MICROELECTRONIC APPLICATIONS AND PROCESS FOR FORMING THE STRUCTURES**

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(22) Filed: **Nov. 21, 2001**

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(60) Provisional application No. 60/091,691, filed on Jun. 30, 1998, and provisional application No. 60/114,512, filed on Dec. 31, 1998.

(51) **Int. Cl.**[7] **H01L 27/082**; H01L 27/102; H01L 29/70; H01L 31/11

(52) **U.S. Cl.** **257/586**; 257/661

(58) **Field of Search** 257/33, 37, 586, 257/661, 662, 663, 750, 758, 759, 760, 501

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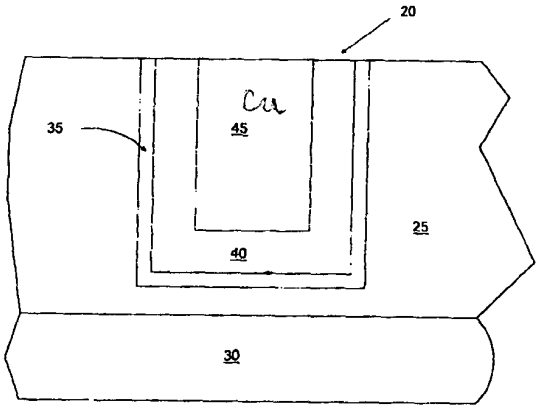
(57) **ABSTRACT**

A metallized structure for use in a microelectronic circuit is set forth. The metallized structure comprises a dielectric layer, an ultra-thin film bonding layer disposed exterior to the dielectric layer, and a low-Me concentration, copper-Me alloy layer disposed exterior to the ultra-thin film bonding layer. The Me is a metal other than copper and, preferably, is zinc. The concentration of the Me is less than about 5 atomic percent, preferably less than about 2 atomic percent, and even more preferably, less than about 1 atomic percent. In a preferred embodiment of the metallized structure, the dielectric layer, ultra-thin film bonding layer and the copper-Me alloy layer are all disposed immediately adjacent one another. If desired, a primary conductor, such as a film of copper, may be formed exterior to the foregoing layer sequence. The present invention also contemplates methods for forming the foregoing structure as well as electroplating baths that may be used to deposit the copper-Me alloy layer.

46 Claims, 14 Drawing Sheets



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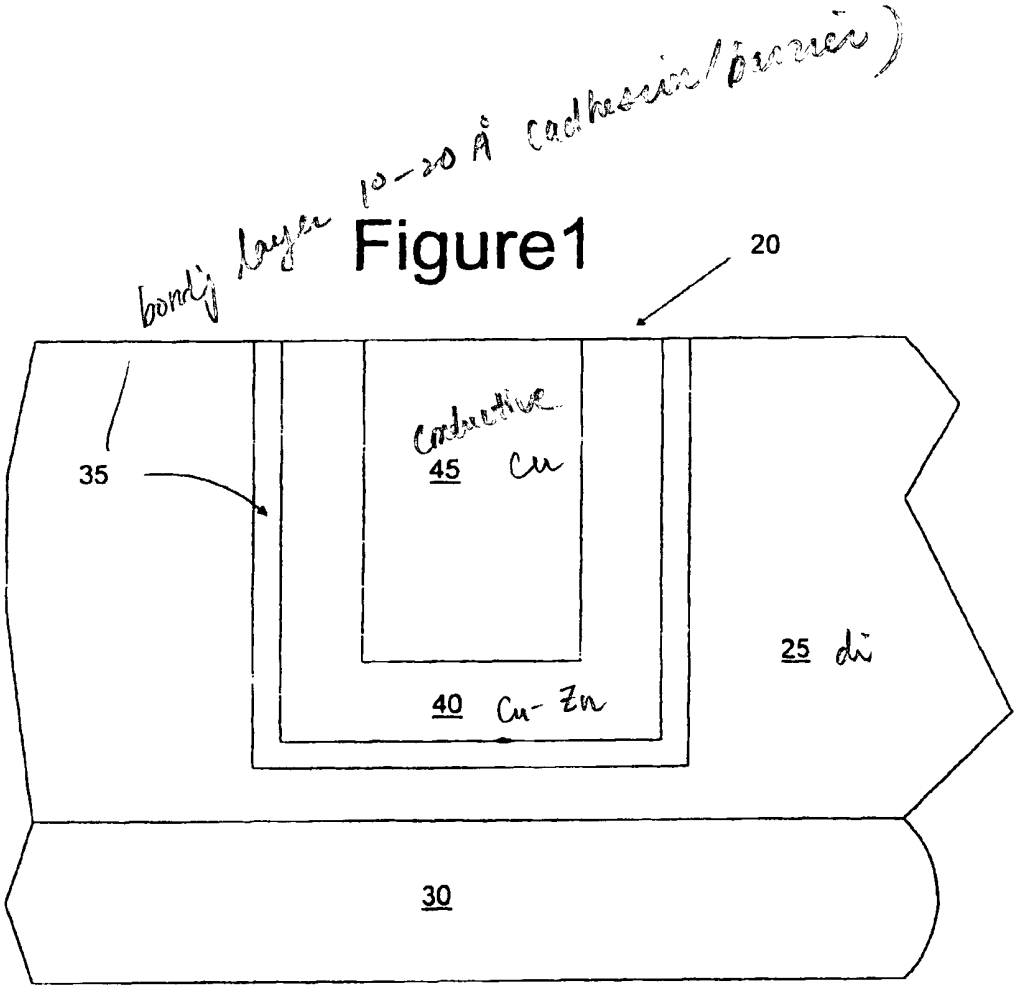
bonding layer 10-20 Å (adhesion/barrier)
20
35
conductive
45 Cu
25 di
40 Cu-Zn
30

Figure1

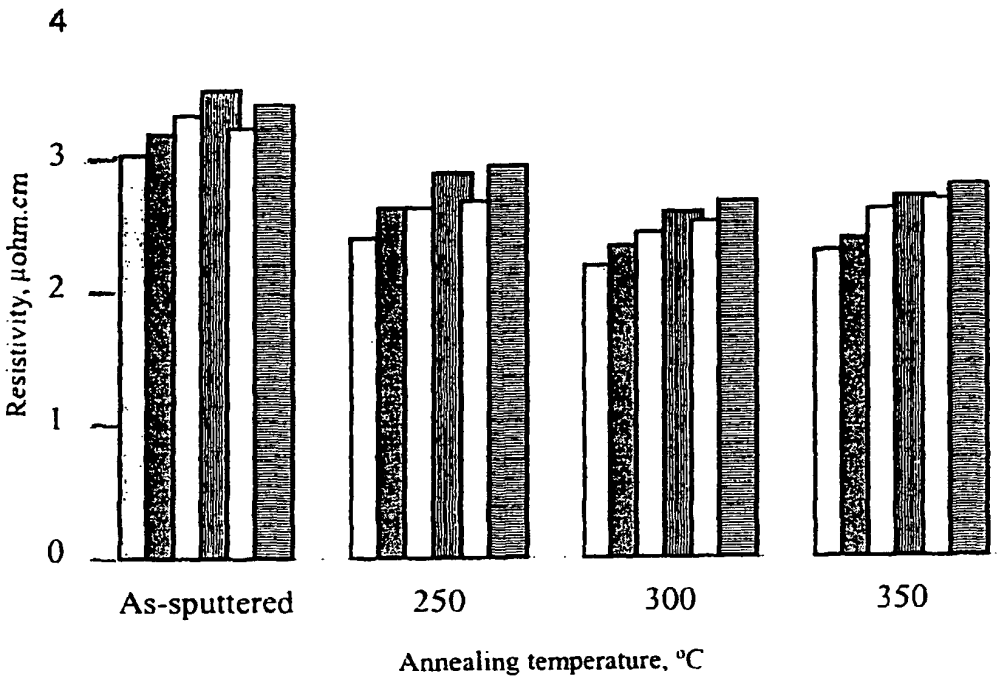
4
3
2
1
0
Resistivity, μohm.cm
As-sputtered
250
300
350
Annealing temperature, °C

FIGURE 2

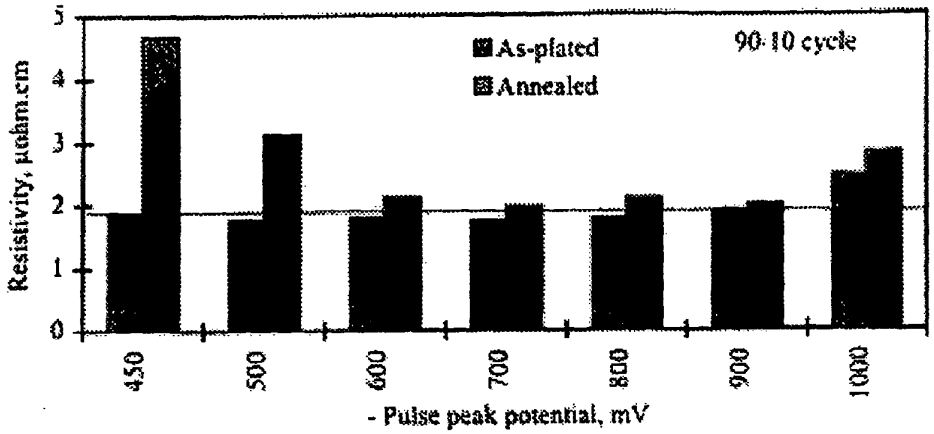

Figure 3A

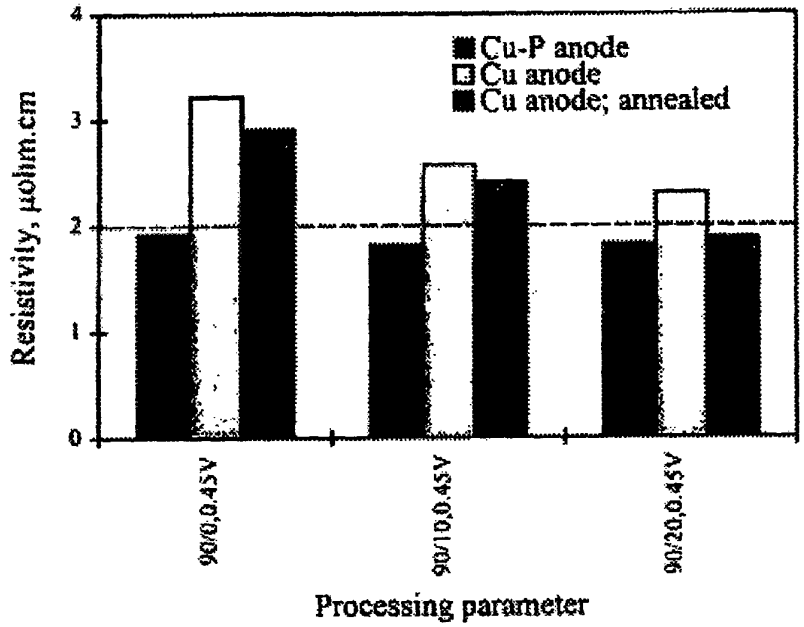

Figure 3B

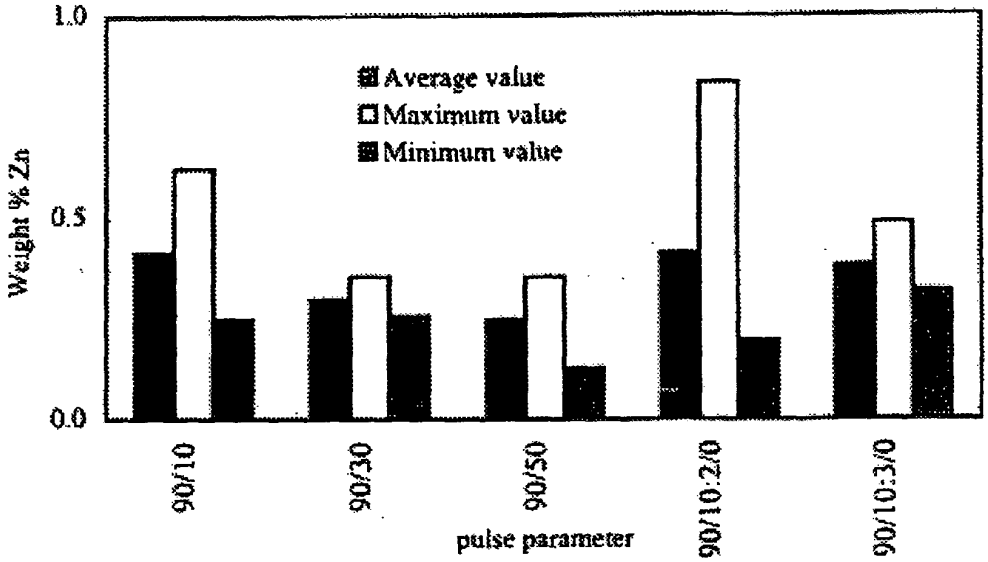
1.0
0.5
0.0
Weight % Zn
Average value
Maximum value
Minimum value
90/10
90/30
90/50
90/10:2/0
90/10:3/0
pulse parameter

Figure 4

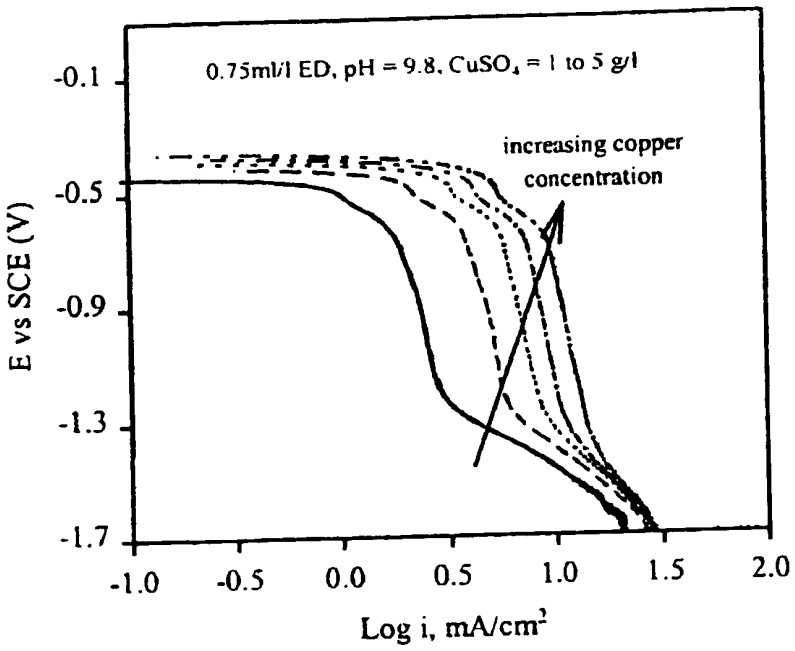

Figure 5 : Polarization curves in test solutions containing 45 g/l $ZnSO_4$ and 0 to 5 g/l $CuSO_4$

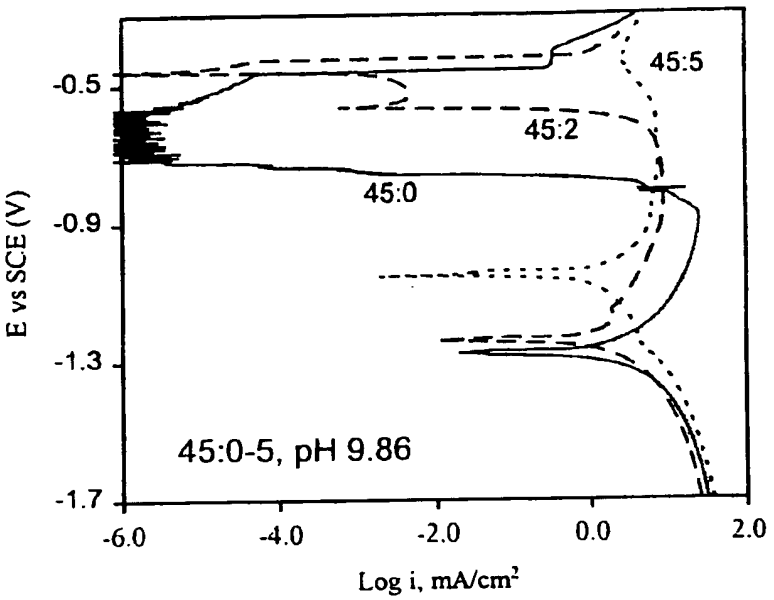

Figure 6 : Polarization curves in test solutions containing 45 g/l $ZnSO_4$ and 0 to 5 g/l $CuSO_4$

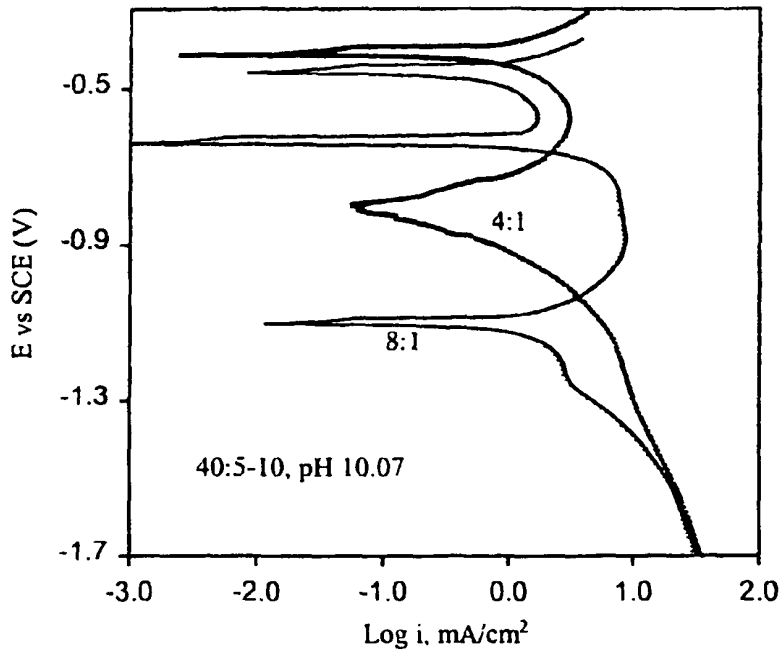

Figure 7 : Polarization curves in test solutions containing 40 g/l $ZnSO_4$ and 5 - 10 g/l $CuSO_4$

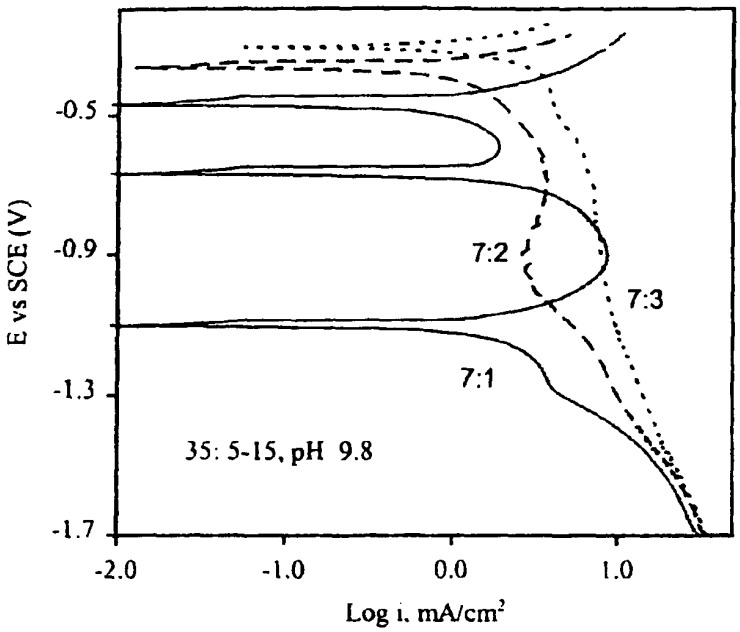

Figure 8 : Polarization curves in test solutions containing 35 g/l $ZnSO_4$ and 5 - 15 g/l $CuSO_4$

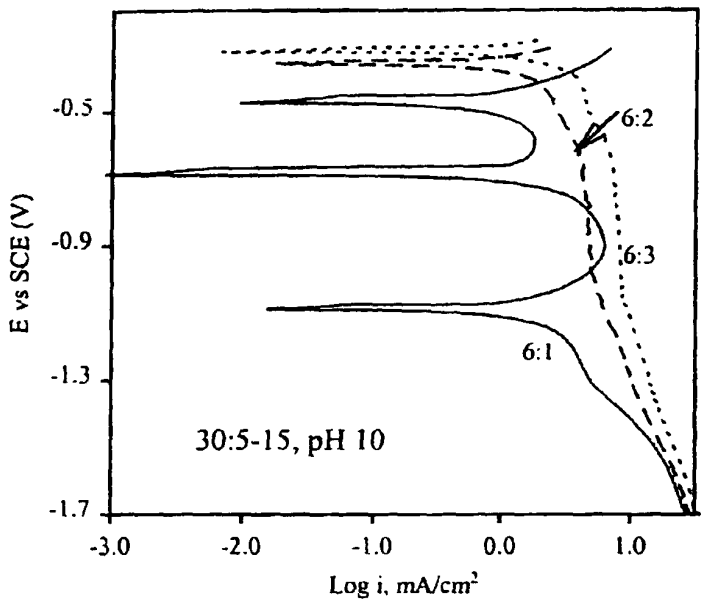

Figure 9 : Polarization curves in test solutions containing 30 g/l $ZnSO_4$ and 5 - 15 g/l $CuSO_4$

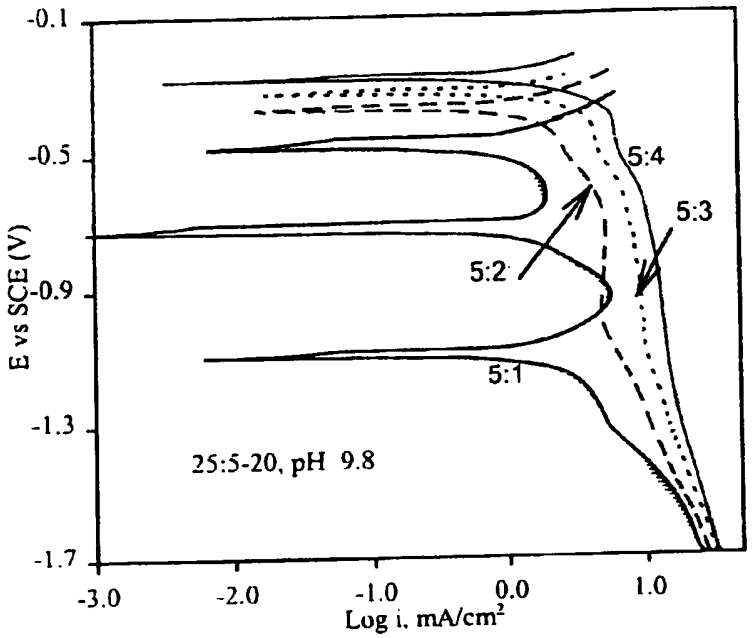

Figure 10: Polarization curves in test solutions containing 25 g/l $ZnSO_4$ and 5 - 20 g/l $CuSO_4$

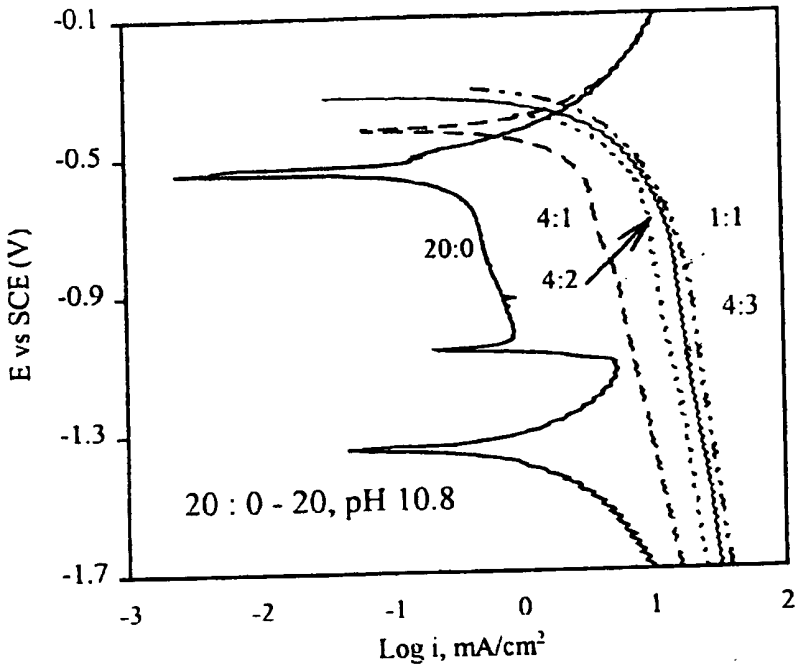

Figure 11: Polarization curves in test solutions containing 20 g/l $ZnSO_4$ and 0 - 20 g/l $CuSO_4$

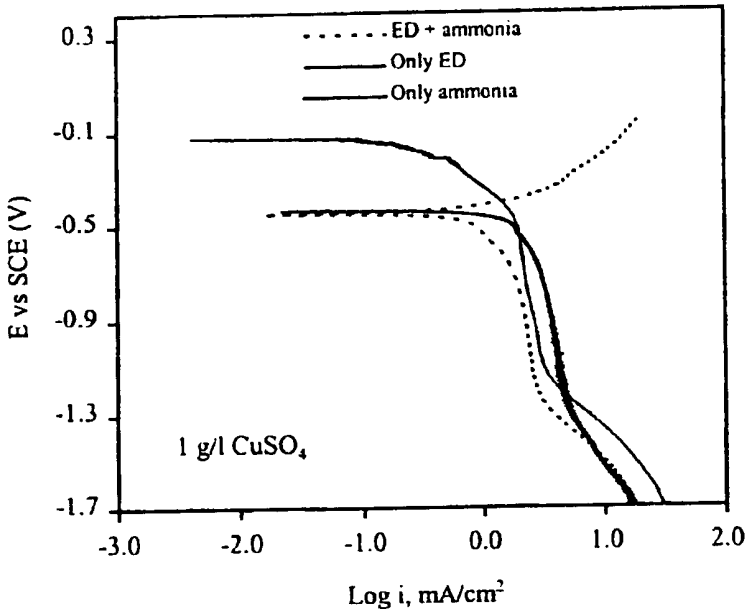

Figure 12 : Polarization curves showing the effect of ammonia and ethylene diamine

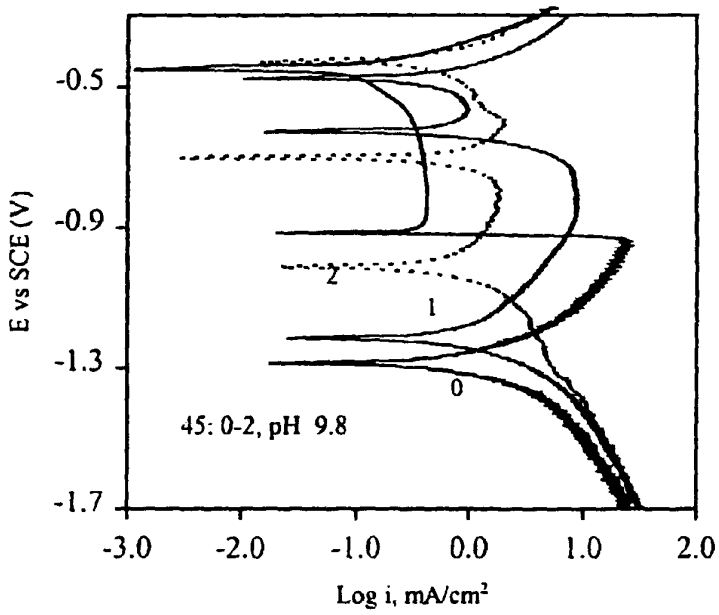

Figure 13 : Polarization curves showing the effect of addition of small quantities of copper

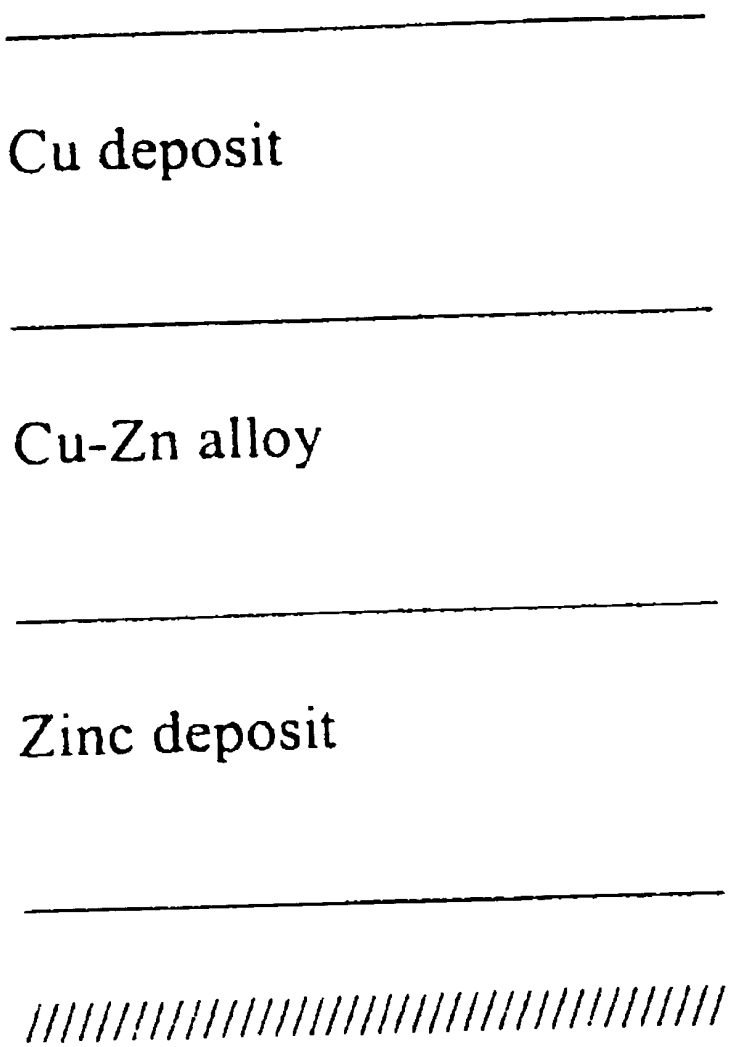

Figure 14

METALLIZATION STRUCTURES FOR MICROELECTRONIC APPLICATIONS AND PROCESS FOR FORMING THE STRUCTURES

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a divisional application of U.S. application Ser. No. 09/386,188, filed Aug. 31, 1999, which is a continuation application of International PCT Patent Application No. PCT/US99/14939, designating the U.S., filed Jun. 30, 1999, and published in English under PCT Article 21(2), which claims priority from U.S. patent application Ser. No. 60/091,691, filed Jun. 30, 1998, and U.S. patent application Ser. No. 60/114,512, filed Dec. 31, 1998.

BACKGROUND OF THE INVENTION

An integrated circuit is an interconnected ensemble of devices formed within a semiconductor material and within a dielectric material that overlies a surface of the semiconductor material. Devices which may be formed within the semiconductor material include MOS transistors, bipolar transistors, diodes and diffused resistors. Devices which may be formed within the dielectric include thin-film resistors and capacitors. Typically, more than 100 integrated circuit die (IC chips) are constructed on a single 8 inch diameter silicon wafer. The devices utilized in each dice are interconnected by conductor paths formed within the dielectric. Typically, two or more levels of conductor paths, with successive levels separated by a dielectric layer, are employed as interconnections. The metallization used to form such interconnects likewise has applicability in the formation of discrete microelectronic components, such as read/write heads, on other substrate materials. In current practice, an aluminum alloy and silicon oxide are typically used for, respectively, the conductor and dielectric.

Delays in propagation of electrical signals between devices on a single dice limit the performance of integrated circuits. Such delays in propagation also limit the performance of discrete microelectronic components. More particularly, these delays limit the speed at which an integrated circuit or microelectronic component may process or otherwise conduct these electrical signals. Larger propagation delays reduce the speed at which the integrated circuit may process the electrical signals, while smaller propagation delays increase this speed. Accordingly, integrated circuit manufacturers seek ways in which to reduce the propagation delays.

For each interconnect path, signal propagation delay may be characterized by a time delay τ. See E. H. Stevens, *Interconnect Technology*, QMC, Inc., July 1993. An approximate expression for the time delay, τ, as it relates to the transmission of a signal between transistors on an integrated circuit is given by the equation:

$$\tau = RC[1+(V_{SAT}/RI_{SAT})]$$

In this equation, R and C are, respectively, an equivalent resistance and capacitance for the interconnect path, and I_{SAT} and V_{SAT} are, respectively, the saturation (maximum) current and the drain-to-source potential at the onset of current saturation for the transistor that applies a signal to the interconnect path. The path resistance is proportional to the resistivity, ρ, of the conductor material. The path capacitance is proportional to the relative dielectric permittivity, K_e, of the dielectric material. A small value of τ requires that the interconnect line carry a current density sufficiently large to make the ratio V_{SAT}/RI_{SAT} small. It follows, therefore, that a low-ρ conductor that can carry a high current density and a low-K_e dielectric should be utilized in the manufacture of high-performance integrated circuits.

To meet the foregoing criterion, copper interconnect lines within a low-K_e dielectric will likely replace aluminum-alloy lines within a silicon oxide dielectric as the most preferred interconnect structure. See "Copper Goes Mainstream: Low-k to Follow", *Semiconductor International*, November 1997, pp. 67–70. Resistivities of copper films are in the range of 1.7 to 2.0 $\mu\Omega$cm. while resistivities of aluminum-alloy films are higher in the range of 3.0 to 3.5 $\mu\Omega$cm.

Despite the advantageous properties of copper, several problems must be addressed for copper interconnects to become viable in large-scale manufacturing processes.

Diffusion of copper is one such problem. Under the influence of an electric field, and at only moderately elevated temperatures, copper moves rapidly through silicon oxide. It is believed that copper also moves rapidly through low-K_e dielectrics. Such copper diffusion causes failure of devices formed within the silicon.

Another problem is the propensity of copper to oxidize rapidly when immersed in aqueous solutions or when exposed to an oxygen-containing atmosphere. Oxidized surfaces of the copper are rendered non-conductive and thereby limit the current carrying capability of a given conductor path when compared to a similarly dimensioned non-oxidized copper path.

A still further problem with using copper in integrated circuits is that it is difficult to use copper in a multi-layer, integrated circuit structure with dielectric materials. Using traditional methods of copper deposition, copper adheres only weakly to dielectric materials.

Finally, because copper does not form volatile halide compounds, direct plasma etching of copper cannot be employed in fine-line patterning of copper. As such, copper is difficult to use in the increasingly small geometries required for advanced integrated circuit devices.

The semiconductor industry has addressed some of the foregoing problems and has adopted a generally standard interconnect architecture for copper interconnects. To this end, the industry has found that fine-line patterning of copper can be accomplished by etching trenches and vias in a dielectric, filling the trenches and vias with a deposition of copper, and removing copper from above the top surface of the dielectric by chemical-mechanical polishing (CMP). An interconnect architecture called dual damascene can be employed to implement such an interconnect structure and thereby form copper lines within a dielectric.

At least one of the processes in the formation of the dual-damascene architecture is particularly troublesome. More particularly, deposition of thin, uniform barrier and seed layers into high aspect ratio (depth/diameter) vias and high aspect ratio (depth/width) trenches is difficult. The upper portions of such trenches and vias tend to pinch-off before the respective trench and/or via is completely filled or layered with the desired material. This problem is further exacerbated when the interconnect structures formed in the trenches and vias include multiple layers. Conductivities of known barrier materials are negligible compared to the conductivity of copper; thus the conductance of narrow interconnect lines is markedly reduced by the barrier layer that must be interposed between the copper and dielectric.

The present inventors have found that deposition of lean alloys of copper may solve these problems. More

particularly, the present inventors have determined that addition of zinc to copper in very low quantities assists in solving the diffusion and self-passivation problems and, further, have suggested a metallization structure that takes advantage of these qualities. Still further, the present inventors have developed an electroplating process that may be used to deposit the copper/zinc alloy that may be used in conjunction with the other processes employed to form the proposed metallization structure.

BRIEF SUMMARY OF THE INVENTION

A metallized structure for use in a microelectronic circuit is set forth. The metallized structure comprises a dielectric layer, an ultra-thin film bonding layer disposed exterior to the dielectric layer, and a low-Me concentration, copper-Me alloy layer disposed exterior to the ultra-thin film bonding layer. The Me is a metal other than copper and, preferably, is zinc. The concentration of the Me is less than about 5 atomic percent, preferably less than about 2 atomic percent, and even more preferably, less than about 1 atomic percent. In a preferred embodiment of the metallized structure, the dielectric layer, ultra-thin film bonding layer and the copper-Me alloy layer are all disposed immediately adjacent one another. If desired, a primary conductor, such as a film of copper, may be formed exterior to the foregoing layer sequence. The present invention also contemplates methods for forming the foregoing structure as well as electroplating baths that may be used to deposit the copper-Me alloy layer.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

FIG.1 illustrates a multilayer metallization structure constructed in accordance with one embodiment of the present invention.

FIG. 2 is a chart showing the relationship between the resistivity of a copper-zinc alloy layer as a function of the annealing temperature.

FIGS. 3A and 3B are charts illustrating the effect of pulse parameters on the resistivity of an electrochemically deposited copper-zinc alloy layer that has been deposited using an electroplating solution having a constituent composition in accordance with one embodiment of the present invention.

FIG. 4 is a chart illustrating the effect of pulse parameters on the zinc composition of an electrochemically deposited copper-zinc alloy that has been deposited using an electroplating solution having a constituent composition in accordance with one embodiment of the present invention.

FIG. 5 is a graph illustrating the polarization behavior of a copper rod in copper sulfate solutions.

FIGS. 6–11 are graphs illustrating the cathodic polarization of a copper rod in plating solutions containing various quantities of zinc and copper sulfate.

FIG. 12 is a graph illustrating the polarization response of copper in a solution containing 1 g/l of copper sulfate and others solution constituents.

FIG. 13 is a graph illustrating polarization curves for plating solutions containing 45 g/l $ZnSO_4$ and various quantities of $CuSO_4$.

FIG. 14 illustrates the composition of an electrochemically deposited layer that was deposited on a copper rod in tests conducted with one embodiment of the disclosed alloy electroplating solution.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 illustrates a multilayer metallization structure constructed in accordance with one embodiment of the present invention. As illustrated, the metallization structure, shown generally at **20**, comprises a plurality of thin layers of conductive material deposited exterior to and, preferably, directly on a dielectric layer **25**. In the specific embodiment shown here, the dielectric layer **25** is disposed exterior to and, preferably, on a substrate **30**, such as a silicon semiconductor wafer. It will be recognized that the metallization structure **20** may be disposed exterior to a wide range of thin film layer and/or substrate material types and, further, may be constructed to conform to various surface geometries. The metallization structure **20** thus has applicability to diverse classes of microelectronic components and/or interconnects.

The composition of the dielectric layer **25** is generally dependent on the function of the metallization structure **20**. When the metallization structure **20** is used to implement a post or line of an electrical interconnect network, the dielectric layer **25** is preferably comprised of a lowK material. When the metallization structure is used to implement a discrete microelectronic component such as a capacitor, however, the dielectric layer **25** is preferably comprised of a highK material. To increase adhesion between the dielectric layer **25** and a subsequent layer, such as ultra-thin bonding layer **35**, the surface of the dielectric layer may be subject to an adhesion promoting process. For example, the dielectric surface may be subject to treatment in an atmosphere having a high ozone content. Alternatively, some form of mild mechanical or chemical abrading process may be used.

As shown in FIG. **1**, the metallization structure **20** is comprised of an ultra-thin film bonding layer **35** disposed exterior to the dielectric layer **25**, a low-zinc concentration, copper-zinc alloy layer **40** disposed exterior to the ultra-thin film bonding layer **35**, and an optional primary conductive layer **45** disposed exterior to the copper-zinc alloy layer **40**. In a preferred embodiment illustrated here in FIG. **1**, each of the layers **35**, **40** and **45** are immediately adjacent one another. As such, the copper-zinc alloy layer **40** is deposited directly on the bonding layer **35** and the optional primary conductive layer **45** is deposited directly on the copper-zinc alloy layer **40**.

In view of the properties of the copper-zinc alloy layer **40**, it becomes possible to use an ultra-thin bonding layer **35**. Preferably, the thickness of the bonding layer **35** is limited to a few monolayers. For example, the bonding layer thickness may be between 10–20 angstroms and, more preferably, less than about 15 angstroms.

The bonding layer **35** functions principally as an adhesion promoter to bond the copper-zinc alloy layer **40** to the dielectric layer **25**. The copper barrier characteristics of the bonding layer material are generally not as important as its bonding characteristics. This is due to the inherent self-passivation and copper-confinement properties of the copper-zinc alloy layer **40**. The present inventors have found that conducting materials that will bond with the dielectric and provide the requisite adhesion will also normally bond well with the copper of the copper-zinc alloy layer **40**. Many such materials, however, have higher resistivities than copper. Since an ultra-thin layer of the bonding material is used, however, the bonding layer **35** does not significantly contribute to the resistance of the multilayer metallization structure **20**. As such, several metals and alloys may be used as the bonding layer material. These include: Al, B, Hf. Ta, Ti, Zn, Cu, Pd, SiC, TiZn, V, Nb, Sb, Sn, nitrides, carbides, borides of refractory metals, and metallic compostructures. Generally stated, the bonding layer material may be any metal or alloy with a high magnitude free-energy of forma-

tion for the compounds that will form at the dielectric-metal interface (e.g. titanium carbide or aluminum oxide forming on a polymer/titanium interface, or silicon oxide/aluminum interface, respectively). Depending on the particular material chosen, the bonding layer **35** may be applied using one or more commonly known deposition techniques, such as PVD or CVD. As technology advances, the bonding layer **35** may ultimately be susceptible to application using an electrochemical deposition process.

The optional primary conducting layer **45** may be deposited on the copper-zinc alloy layer **40** to provide an even lower resistivity material that functions as the primary conductive path for electrical signals and, thus, reduces the overall resistance of the metallization structure **20**. The optional primary conducting layer **45** may not be necessary in situations where the copper-zinc alloy layer **40** has a resistivity that is sufficiently low to meet the circuit or component requirements. The conducting layer **45** of the illustrated embodiment, in most applications, is preferably copper. The copper layer may be deposited using any of the known film deposition techniques. However, it is preferably deposited using an electrochemical deposition technique.

One of the unique layers employed in the metallization structure **20** is the copper-zinc alloy layer **40**. The copper-zinc alloy layer **40** includes a very low zinc content. Preferably, the zinc content is below about 5 atomic percent. More preferably, the zinc content is below about 2 atomic percent. The present inventors have found that even those copper-zinc alloys having a zinc content below about 1 atomic percent exhibit properties that make them suitable for inclusion in the metallization structure **20**. A balanced approach to choosing the zinc content is generally necessary. The greater the zinc content in the alloy, the greater is the resistivity of the resulting layer. To reduce the resistivity of the alloy layer, the zinc content of the alloy should be minimized. However, with reduced zinc content, the oxidation resistance and copper-confinement properties begin to degrade. As such, the zinc content should be chosen to balance the resistivity of the layer against the oxidation resistance and copper-confinement properties. The zinc content chosen for the alloy thus becomes dependent on the performance requirements of the metallization structure **20**.

It is the properties of the copper-zinc alloy layer **40** that allow it to be used in conjunction with the very thin bonding layer **35**. By using an ultra-thin bonding layer, microstructures that are filled using the sequence of layers of metallization structure **20** include a larger proportion of high-conductivity to low-conductivity materials than can be obtained when using the thicker bonding/barrier layers that are necessary when a pure copper layer is employed without an intermediate copper-zinc alloy layer.

The copper-zinc alloy layer **40** may be deposited using sputtering techniques or, as will be set forth in greater detail below, electrochemical deposition techniques. When the layer **40** is sputter deposited, the alloy composition is generally determined by the composition of the target. Alloy layers having different zinc content are thus generally sputter deposited using different copper-zinc composition targets.

Notwithstanding the particular deposition technique used to deposit the layer, the present inventors have found that the resistivity of the copper-zinc alloy layer **40** may be reduced using a low-temperature annealing process. FIG. **2** is a chart showing the relationship between the resistivity of a copper-zinc alloy layer as a function of the annealing temperature for a number of samples in which the copper-zinc alloy was sputter deposited on the dielectric material. The sputtering was done at 2.5 kW (0.5 k volt×5 amps) with a base pressure of 10^{-7} Torr and an argon pressure of 5 mTorr for 10 minutes. The annealing took place at the given temperatures for a time period of 30 minutes. The sputter target had a zinc content of 5 atomic percent.

As illustrated, annealing under the foregoing conditions generally improved the resistivity of the copper-alloy layer when compared to the resistivity of the layer as originally deposited. The results show a general decrease in resistivity with increasing annealing temperature. However, the resistivity was not significantly enhanced with increasing annealing temperatures above about 350° C.–400° C. As such, given the diminishing resistivity enhancement provided above such temperatures, it has been found to be preferable to anneal the copper-zinc alloy layer at an annealing temperature that is at or below this temperature range, thereby increasing the available thermal budget of the microelectronic workpiece (e.g., a semiconductor wafer). The annealing process may take place at an even lower temperature when one or more of the layers of the overall microelectronic workpiece degrade or are otherwise stressed when subject to high annealing temperatures. For example, many low-K dielectric materials begin to degrade at temperatures above about 250 °.C.–350° C. As such, annealing must take place below such temperatures.

Although the copper-zinc alloy layer **40** may be deposited using a sputter deposition process, acid copper electroplating is becoming popular and it has a number of advantages over other types of deposition. It is relatively fast, inexpensive, easy to maintain and control, less toxic and produces deposits of good uniformity, strength and ductility. Copper and zinc, however, are widely separated in electrochemical series ($E_{Cu/Cu2+}$=+0.34 and $E_{Zn/Zn2+}$=−0.76 mV with respect to Standard Hydrogen Electrode, SHE). In an acid medium, where both metals exist as simple cations, namely Cu^{2+} and Zn^{2+}, it is therefore not possible to co-deposit both copper and zinc. When an attempt is made to electrochemically deposit two different metals having different deposition potentials from an electroplating solution, the metal having the lower magnitude deposition potential will generally plate out from the solution and a significant amount of gas will evolve before reaching the greater magnitude deposition potential of the other metal. So it therefore becomes necessary to think of chemicals, which when added to a system containing simple cations, bring the disparate deposition potentials proximate one another so that the metals can be co-deposited. To this end, complexing agents (coordinating ligands) such as cyanide, ethylenediamine, EDTA etc., may be used. These ligands coordinate with copper ions and form what are called coordinate complexes of copper thereby reducing the activity of copper and, hence, the electrode potentials. In other words, in the presence of complexing agents, the reduction potentials and, thus, the potentials at which the metals are electrodeposited, are shifted to more negative regions. The extent to which they are shifted is different for different elements. The present inventors have exploited this phenomenon to electroplate a thin film copper layer with very small amounts of zinc of less than 5 atomic percent and, more preferably, around about 1 atomic percent, and below.

To facilitate the electroplating of both copper and zinc to form the copper-zinc alloy layer **40**, a unique electroplating solution for electrochemically depositing a copper-zinc alloy was developed. The preferred solution may be used in the electrochemical deposition of the copper-zinc alloy layer **40** of the metallization structure **20** shown in FIG. **1**, as well as

in the electrochemical deposition of other copper-based alloys used for the alloy layer **40** of structure **20**. In accordance with a preferred composition of the solution, the solution includes the following constituents:

TABLE 1

PREFERRED ELECTROPLATING SOLUTION

CONSTITUENT	CONCENTRATION	FUNCTION
$MeSO_4$	10–40 g/l	Used as a source of metal, Me, that is to be alloyed with the copper (Me = zinc, aluminum, boron, magnesium, Ce, etc.)
$CuSO_4$	5–20 g/l	Used as a source of copper for the metal alloy
$(NH_4)_2SO_4$	20–40 g/l	Used as a complexing agent
Addition agent	0.1–1 ml/l	Preferably, ED or EDTA, serving as both a wetting agent as well as a complexing agent (optional constituent)
NH_4OH	50–100 ml/l	Used to adjust the pH of the solution, which should be maintained between a pH of about 8 to a pH of about 11. This constituent also functions as a complexing agent.

With the foregoing solution, it is possible to use a wide range of plating parameters to deposit a copper-zinc alloy layer **40** having a low resistivity (e.g., 1.8–2.4 u-ohms/cm) while also having the desired oxidation resistance and copper confinement properties. Preferably, the alloy is plated using a constant potential (a. opposed to a constant current) waveform. The plating potential used is preferably between 300 mV and 900 mV cathodic. Although a DC plating waveform may be used, it is preferable to have a forward pulsed waveform. The forward pulsed waveform may have an on/off cycle of 50/20 msec to 90/10 msec. Particularly good via and trench microstructure filling results when a waveform of 0.6/0.3 msec is used.

FIGS. **3A** and **3B** are charts illustrating the effect of pulse parameters on the resistivity of the resulting copper-zinc alloy layer, while FIG. **4** is a chart illustrating the effect of pulse parameters on the zinc composition of the resulting layer. The rightmost pulse parameter results illustrated in of each of the figures included plating waveforms having reverse pulses as well as forward pulses. As can be seen from FIG. **4**, the zinc content of the alloy may be manipulated by varying the pulse parameters.

Although an inert anode may be used in the deposition process, a consumable anode is preferred. The consumable anode may be comprised of pure copper or of copper-phosphorous, with the copper-phosphorus anode providing better microstructure filling and better copper-alloy layer characteristics.

Various tests were performed to characterize the particular constituents used in the foregoing electroplating solution. For example, the polarization behavior of a copper rod in copper sulfate solutions is shown in FIG. **5**. Increasing the concentration of copper in the bath shifted the SSP (Steady State Potential) to the anodic side. There did not appear to be any hydrogen evolution in the potential range studied.

The cathodic polarizations of a copper rod in plating solutions containing various quantities of zinc and copper sulfate are illustrated in FIGS. **6–11**. When the ratio of zinc to copper is in the range 8:1 to 5:1, the polarization curves go through three minima, the first one at the highest negative potential corresponds to zinc deposition/dissolution, the other two correspond to a steady state region of alloy of copper and zinc. The increase in copper content in solution shifts the curves upwards to more positive potentials. Though the ratio varies, the total amount of copper in all these examples is the same: 5 g/l. Only when the copper concentration is increased from this level to 10 g/l (in 30:10 combination, where the ratio is 3:1, but total copper sulfate concentration is 10 g/l), do the two minima at negative potentials disappear and leave only one SSP at high positive potential. This is due to the fact that the solution attains a copper dissolution/deposition equilibrium. Two parameters were thus identified: the ratio of copper sulfate to zinc sulfate in solution and the concentration of copper sulfate. Unless the copper concentration is increased above 10 g/l, it does not appear to be possible to avoid the minima at higher negative potentials. By increased addition of copper to zinc sulfate (Ratio 1:1 and copper at 20 g/l level), the current is not increased significantly. This is due to complexation, but there is an advantage of stability of the solution where the concentration decrease due to plating may not change the current density significantly. Thus it is best to utilize a composition that allows the solution to work over a wide range of potentials to obtain the same composition of the deposit.

FIG. **12** shows the polarization response of copper in a solution containing 1 g/l copper sulfate. The presence of ammonium hydroxide induces the formation of aminocomplexes, whereas the addition of ethylene amine induces the formation of ethylene amine complexes of metallic ions present in the solution. Whenever a complex ion is formed (by the reaction of metal ions with coordinating ligands present in solution), the activity of metal ions is reduced and this in turn reduces the deposition potential. The complexation also increases the overpotential and decreases the cathodic current density. These effects can be seen in this polarization curve. When only the amine is present, the steady state potential is around –1 V (SCE). Thus at potentials more negative to this, deposition of copper is possible. When ammonium hydroxide is present in test solution, the SSP is depressed to a higher negative value, to –0.47 V(SCE). This indicates that the complex formed with ammonia can be reduced only at higher negative potentials. The following equations represent the sequence of reactions that lead to the deposition of copper from complexes.

$$Cu^{2+}+4NH_3 \rightarrow [Cu(NH_3)_4]^{2+}$$

$$[Cu(NH_3)_4]^{2+}+2e^- \rightarrow Cu+NH_3$$

$$Cu_{2+}+ED \rightarrow [Cu(ED)_2]^{2+}$$

$$[Cu(ED)_2]^{2+}+2e^- \rightarrow Cu+2ED$$

FIG. **13** illustrates the potentiodynamic polarization curves in plating solutions containing 45 g/l $ZnSO_4$ and various quantities of $CuSO_4$. The curves show active deposition/dissolution regions that correspond to that of zinc, copper and/or an alloy of these metals. The reduction of zinc complex to zinc occurred at potentials negative to –1.3 V (SCE) when the bath contained only zinc sulfate and no copper sulfate. The addition of 1 and 2 g/l copper sulfate resulted in this potential shifting to more anodic values, to –1.2 and –1.0 V (SCE) respectively. The steady state region that corresponds to that of pure zinc was masked by the simultaneous copper deposition. The extent to which this

occurred depended on the amount of copper in the bath. Thus even before zinc that deposited at higher potentials dissolved, copper/copper alloy started to deposit. To observe the cross section of the cathodically polarized specimens, the experiment was terminated when the current in the cathodic region went below 100 μA (approximately at −0.5 V SCE). The specimen was then polished to observe the layers from surface to inside. As illustrated in FIG. **14**, the layers were seen to be copper, Cu—Zn alloy and zinc as viewed from from the deposit surface to copper rod/deposit interface.

The electrochemical deposition of the copper-zinc alloy layer **40** may be implemented in a wide range of electroplating reactor types. An integrated processing tool that incorporates one or more electroplating reactors that are particularly suitable for implementing the foregoing electrochemical deposition process is available from Semitool, Inc., of Kalispell, Mont. Such tools are sold under the brand names LT-210™ and Equinox™ and are readily adapted to implement a wide range of electroplating processes used in the fabrication of microelectronic circuits and components. Advantageously, the reactors employed in these tools rotate a workpiece during the electrochemical deposition process, thereby enhancing the uniformity of the resulting film. It is preferable to rotate a workpiece when depositing the copper-zinc alloy layer **40** (or other alloy layer) onto the workpiece. To further enhance the quality of the resulting copper-Zn alloy layer **40**, the electrochemical deposition reaction chamber(s) of these tools may be fitted with an ultrasonic generator that provides ultrasonic energy to the electroplating solution during the electrochemical deposition process to thereby enhance the desired characteristics of the resulting alloy layer.

In addition to electroplating reactors, such tools frequently include other ancillary processing chambers such as, for example, pre-wetting chambers, rinsing chambers, etc., that are used to perform other processes typically associated with electrochemical deposition. Semiconductor wafers, as well as other microelectronic workpieces, are processed in such tools one-by-one in the reactors and are transferred between the processing stations, as well as between the processing stations and input/output stations, by a robotic transfer mechanism. The robotic transfer mechanism, the electroplating reactors and the plating recipes used therein, as well as the components of the processing chambers are all under the control of one or more programmable processing units.

Numerous modifications may be made to the foregoing inventions without departing from the basic teachings thereof. Although the present inventions have been described in substantial detail with reference to one or more specific embodiments, those of skill in the art will recognize that changes may be made thereto without departing from the scope and spirit of the invention as set forth in the appended claims.

What is claimed is:

1. A metallized structure for use in a microelectronic circuit, the metallized structure comprising:

a dielectric layer;

an ultra-thin film bonding layer disposed exterior to the dielectric layer; and

a low-Me concentration, copper-Me alloy layer disposed exterior to the ultra-thin film bonding layer.

2. A metallized structure as set forth in claim **1** wherein the dielectric layer is formed from a low-K dielectric material.

3. A metallized structure as set forth in claim **1** wherein the dielectric layer is formed from a high-K dielectric material.

4. A metallized structure as set forth in claim **1** wherein the Me content of the copper-Me alloy layer is less than or equal to about 5 atomic percent.

5. A metallized structure as set forth in claim **1** wherein the zinc content of the copper-Me alloy layer is less than or equal to about 2 atomic percent.

6. A metallized structure as set forth in claim **1** wherein the zinc content of the copper-Me alloy layer is less than or equal to about 1 atomic percent.

7. A metallized structure as set forth in claim **1** wherein the ultra-thin bonding layer has a thickness between about 10–20 angstroms.

8. A metallized structure as set forth in claim **7** wherein the ultra-thin bonding layer has a thickness of less than about 15 angstroms.

9. A metallized structure as set forth in claim **1** wherein the ultra-thin bonding layer is comprised of a metal.

10. A metallized structure as set forth in claim **1** wherein the ultra-thin bonding layer is comprised of a metal alloy.

11. A metallized structure for use in a microelectronic circuit, the metallized structure comprising:

a dielectric layer;

an ultra-thin film bonding layer disposed exterior to the dielectric layer; and

a low-zinc concentration, copper-zinc alloy layer disposed exterior to the ultra-thin film bonding layer.

12. A metallized structure as set forth in claim **11** and further comprising a primary copper conductor disposed exterior to the low-zinc concentration, copper-zinc alloy layer.

13. A metallized structure as set forth in claim **11** wherein the dielectric layer is formed from a low-K dielectric material.

14. A metallized structure as set forth in claim **11** wherein the dielectric layer is formed from a high-K dielectric material.

15. A metallized structure as set forth in claim **11** wherein the zinc content of the copper-zinc alloy layer is less than or equal to about 5 atomic percent.

16. A metallized structure as set forth in claim **11** wherein the zinc content of the copper-zinc alloy layer is less than or equal to about 2 atomic percent.

17. A metallized structure as set forth in claim **11** wherein the zinc content of the copper-zinc alloy layer is less than or equal to about 1 atomic percent.

18. A metallized structure as set forth in claim **11** wherein the ultra-thin bonding layer has a thickness between about 10–20 angstroms.

19. A metallized structure as set forth in claim **18** wherein the ultra-thin bonding layer has a thickness of less than about 15 angstroms.

20. A metallized structure as set forth in claim **11** wherein the ultra-thin bonding layer is comprised of a metal.

21. A metallized structure as set forth in claim **11** wherein the ultra-thin bonding layer is comprised of a metal alloy.

22. A metallized structure for use in a microelectronic circuit, the metallized structure comprising:

a dielectric layer;

an ultra-thin film bonding layer disposed adjacent to the dielectric layer; and

a low-zinc concentration, copper-zinc alloy layer disposed adjacent to the ultra-thin film bonding layer.

23. A metallized structure as set forth in claim **22** and further comprising a primary copper conductor layer adjacent the low-zinc concentration, copper-zinc alloy layer.

24. A metallized structure as set forth in claim **22** wherein the dielectric layer is formed from a low-K dielectric material.

25. A metallized structure as set forth in claim 22 wherein the dielectric layer is formed from a high-K dielectric material.

26. A metallized structure as set forth in claim 22 wherein the zinc content of the copper-zinc alloy layer is less than or equal to about 5 atomic percent.

27. A metallized structure as set forth in claim 22 wherein the zinc content of the copper-zinc alloy layer is less than or equal to about 2 atomic percent.

28. A metallized structure as set forth in claim 22 wherein the zinc content of the copper-zinc alloy layer is less than or equal to about 1 atomic percent.

29. A metallized structure as set forth in claim 22 wherein the ultra-thin bonding layer has a thickness between about 10–20 angstroms.

30. A metallized structure as set forth in claim 29 wherein the ultra-thin bonding layer has a thickness of less than about 15 angstroms.

31. A metallized structure as set forth in claim 22 wherein the ultra-thin bonding layer is formed from a material with a high magnitude free-energy of formation for compounds that will form at the dielectric-bonding layer interface.

32. A metallized structure as set forth in claim 22 wherein the ultra-thin bonding layer is comprised of a metal.

33. A metallized structure as set forth in claim 22 wherein the ultra-thin bonding layer is comprised of a metal alloy.

34. A metallized structure for use in a microelectronic circuit formed by a process comprising the steps of:

depositing a dielectric layer on the microelectronic workpiece;

depositing an ultra-thin bonding layer over an exterior of the dielectric layer;

depositing a low Me concentration, copper-Me alloy layer exterior to the ultra-thin bonding layer, where Me is a metal other than copper.

35. The metallized structure of claim 34, wherein the ultra-thin bonding layer is disposed immediately adjacent the dielectric layer and the copper-Me alloy layer is disposed immediately adjacent the ultra-thin bonding layer.

36. The metallized structure of claim 35, wherein the concentration of Me is less than about 5 atomic percent.

37. The metallized structure of claim 35, wherein the concentration of Me is less than about 2 atomic percent.

38. The metallized structure of claim 35, wherein the concentration of Me is less than about 1 atomic percent.

39. The metallized structure of claim 35, wherein Me is zinc.

40. The metallized structure of claim 36, wherein Me is zinc.

41. The metallized structure of claim 37, wherein Me is zinc.

42. The metallized structure of claim 38, wherein Me is zinc.

43. The metallized structure of claim 34, wherein the copper-Me alloy layer is deposited using an electrochemical deposition process.

44. The metallized structure of claim 43, wherein the electrochemical deposition process uses a constant potential waveform.

45. The metallized structure of claim 44, wherein the constant potential waveform comprises a forward pulsed waveform.

46. The metallized structure of claim 35, wherein the copper-Me alloy layer is deposited using an electrochemical deposition process.

* * * * *

US006387806B1

(12) **United States Patent**
Wang et al.

(10) **Patent No.: US 6,387,806 B1**
(45) **Date of Patent: May 14, 2002**

(54) **FILLING AN INTERCONNECT OPENING WITH DIFFERENT TYPES OF ALLOYS TO ENHANCE INTERCONNECT RELIABILITY**

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(73) Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/655,700**

(22) Filed: **Sep. 6, 2000**

(51) **Int. Cl.**[7] **H01L 21/44**

(52) **U.S. Cl.** **438/687**; 438/637; 438/660; 438/672; 438/675

(58) **Field of Search** 438/694, 643, 438/637, 638, 640, 672, 308, 378, 687, 648, 689, 690, 691, 692, 660, 674, 675, 677

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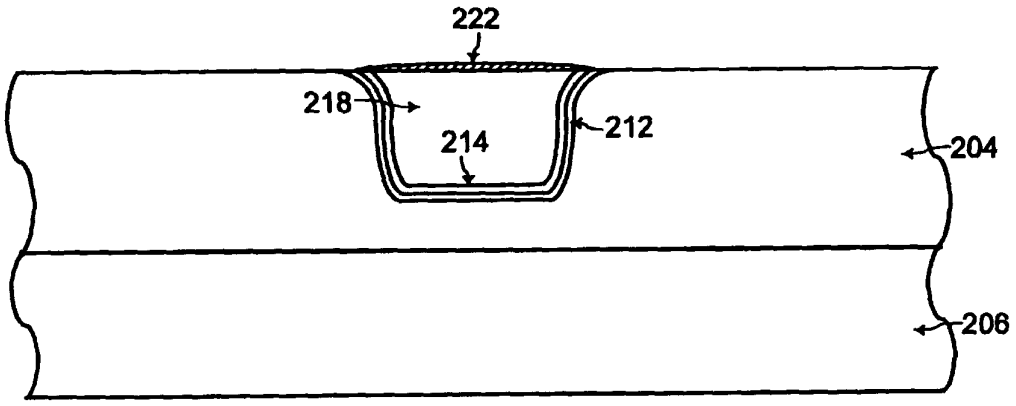
Primary Examiner—Matthew Smith
Assistant Examiner—Victor Yevsikov

(74) *Attorney, Agent, or Firm*—Monica H. Choi

(57) **ABSTRACT**

An interconnect opening of an integrated circuit is filled with a conductive fill, such as copper, with the interconnect opening being within an insulating layer on a semiconductor wafer. A seed layer of a first alloy is deposited conformally onto sidewalls and a bottom wall of the interconnect opening. The first alloy is comprised of a first metal dopant in a bulk conductive material. The first metal dopant has a relatively high solid solubility in the bulk conductive material, and the first metal dopant has a concentration in the bulk conductive material of the seed layer that is lower than the solid solubility of the first metal dopant in the bulk conductive material. At least a portion of the conductive fill grown from the seed layer is comprised of a second alloy with a second metal dopant having a relatively low solid solubility in the bulk conductive material, and the second metal dopant has a concentration in the conductive fill that is higher than the solid solubility of the second metal dopant in the bulk conductive material. A thermal anneal is performed to form an additional encapsulating material that covers a top surface of the conductive fill, and the additional encapsulating material is formed from the second metal dopant diffusing out of the conductive fill during the thermal anneal. A layer of bulk passivation material is formed over the additional encapsulating material and the insulating layer. Use of the first alloy of the seed layer prevents agglomeration of the bulk conductive material of the seed layer at the sidewalls of the interconnect opening. The additional encapsulating material prevents drift of material from the conductive fill along the bottom surface of the layer of bulk passivation material and into the surrounding insulating layer.

16 Claims, 8 Drawing Sheets



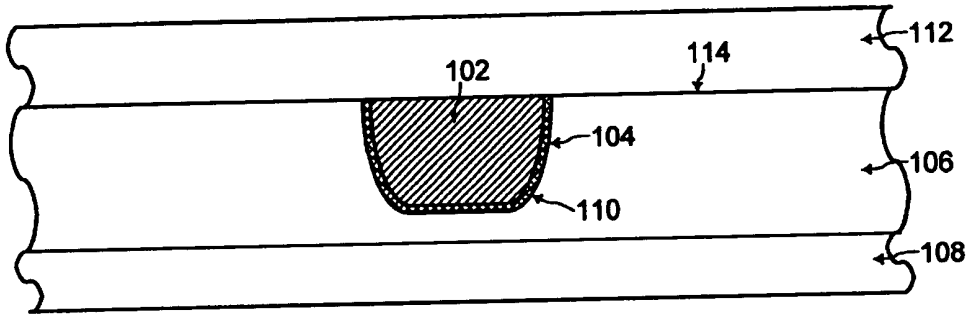


FIG. 1 (Prior Art)

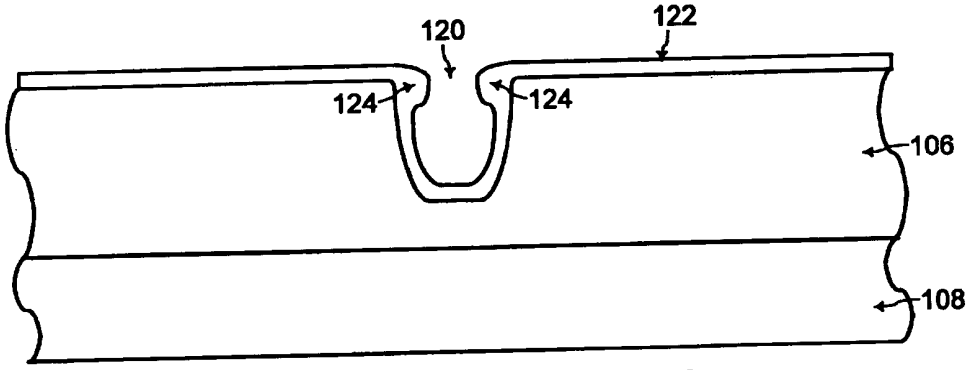


FIG. 2 (Prior Art)

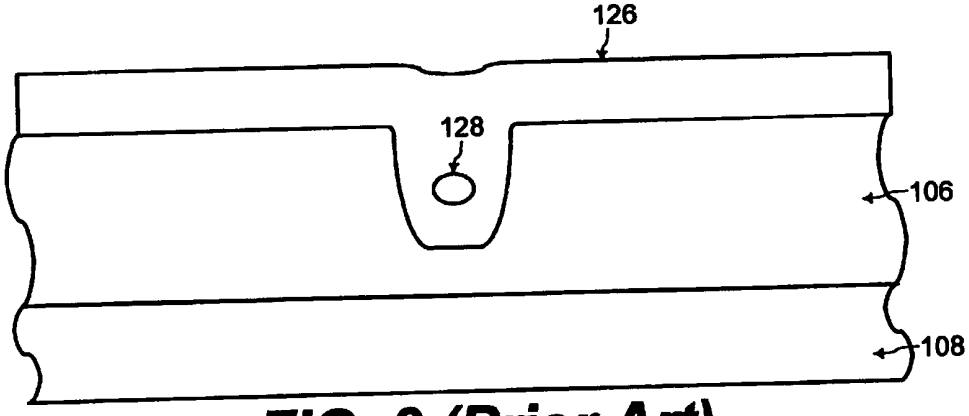


FIG. 3 (Prior Art)

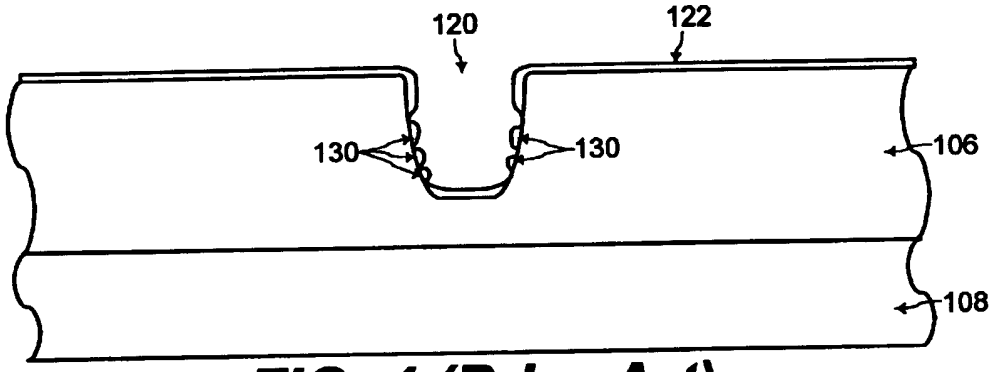


FIG. 4 (Prior Art)

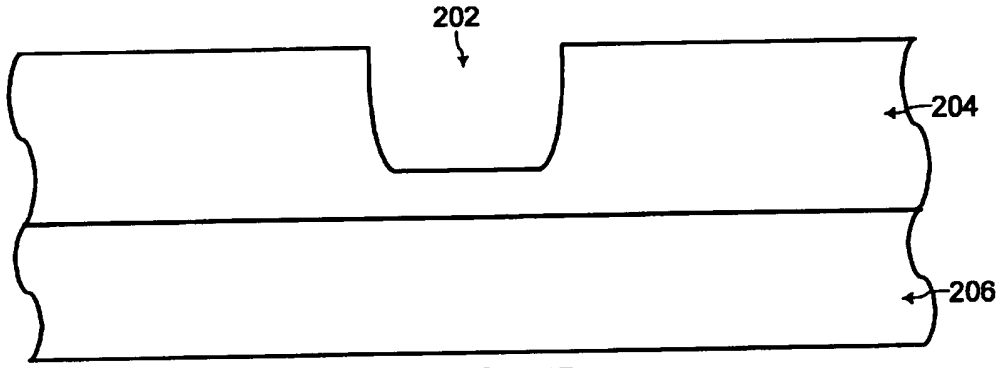


FIG. 5

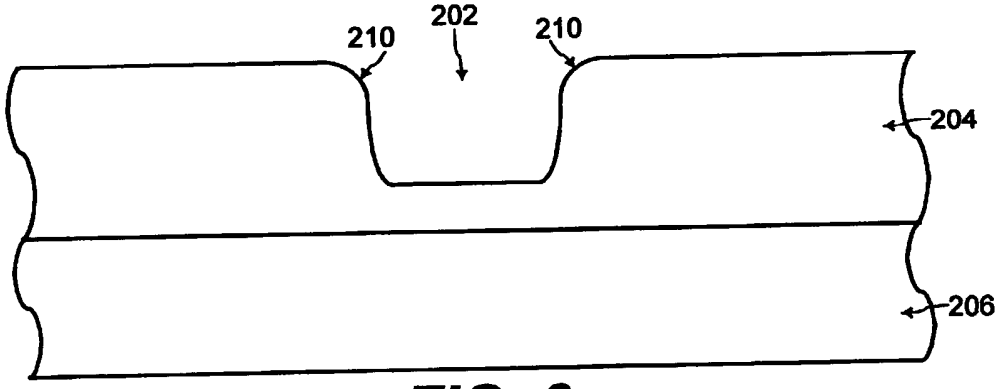


FIG. 6

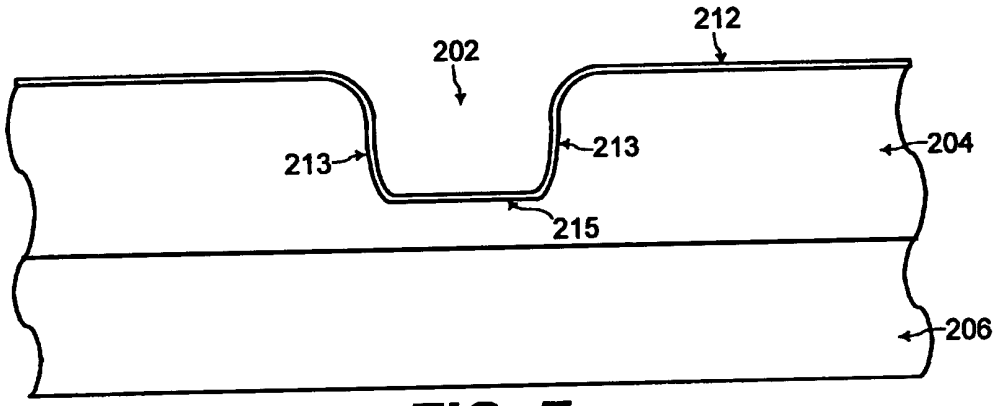


FIG. 7

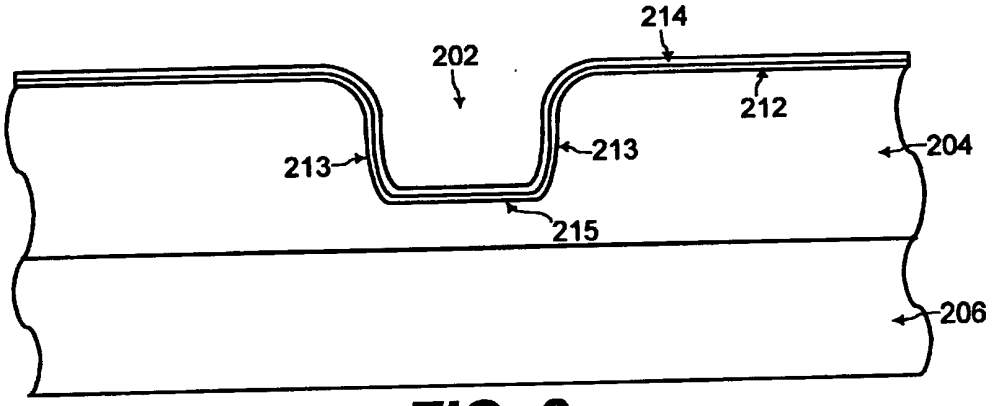


FIG. 8

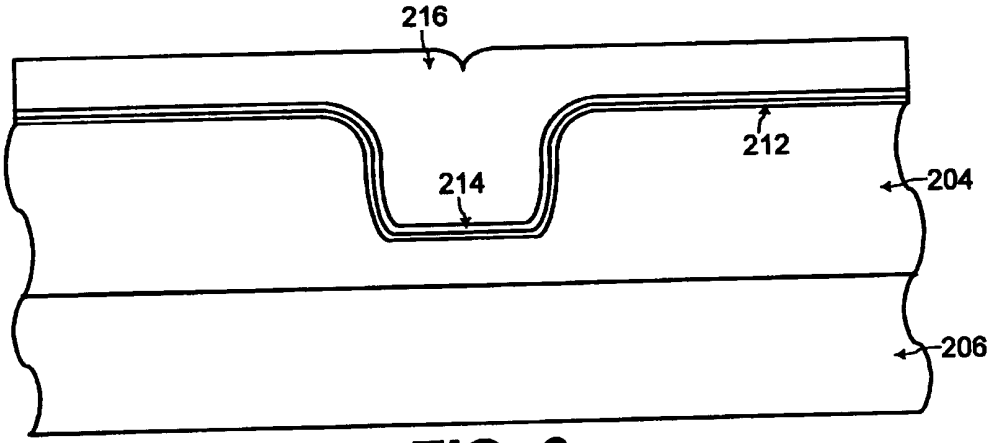


FIG. 9

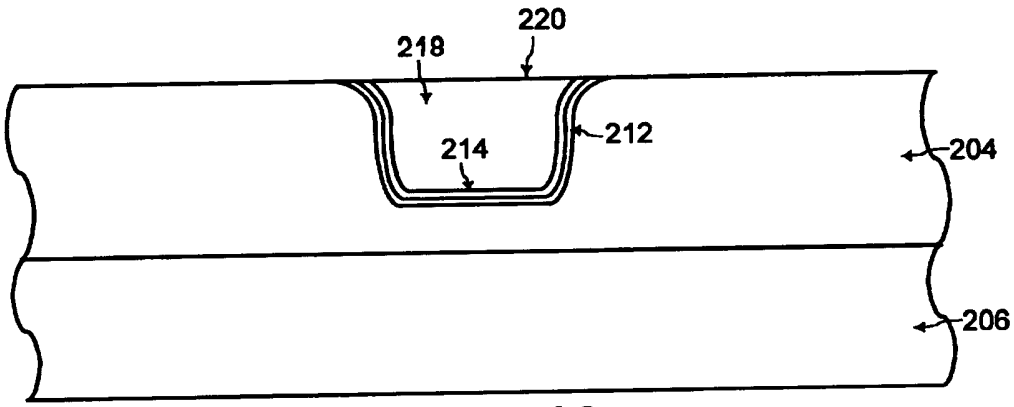


FIG. 10

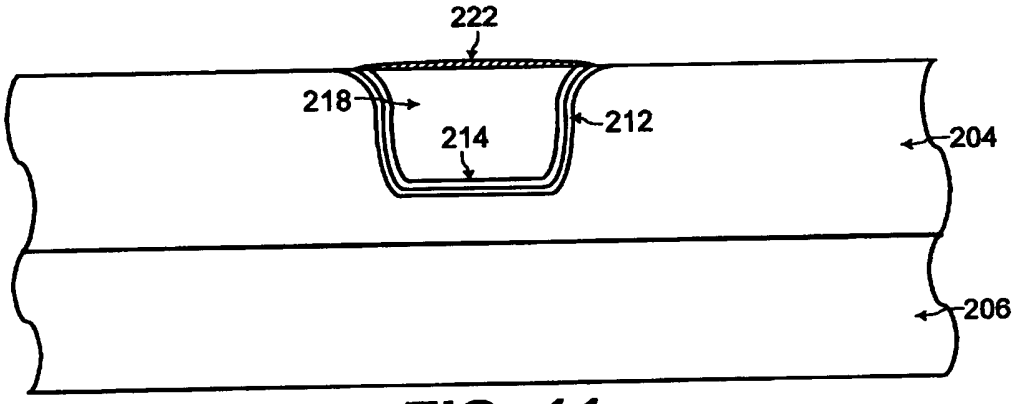


FIG. 11

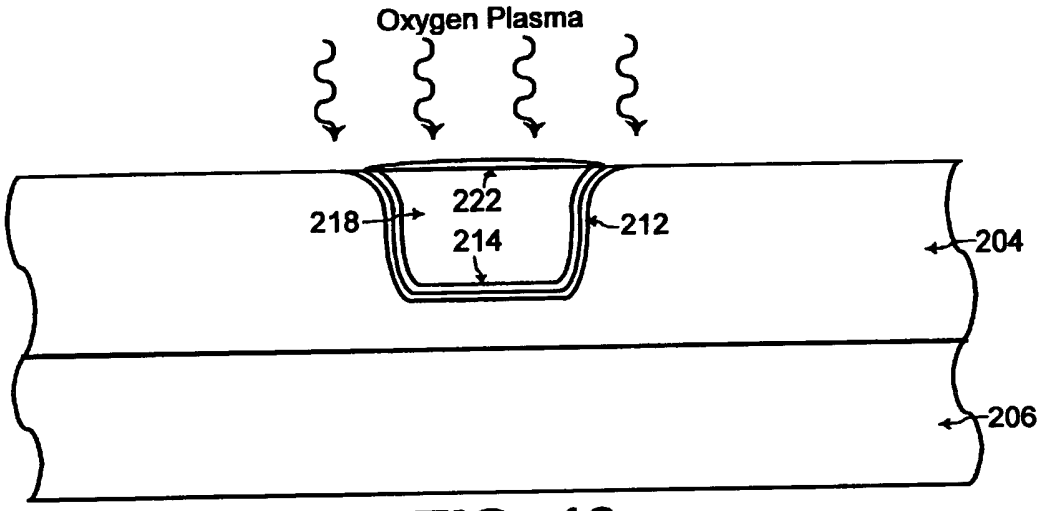

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FIG. 12

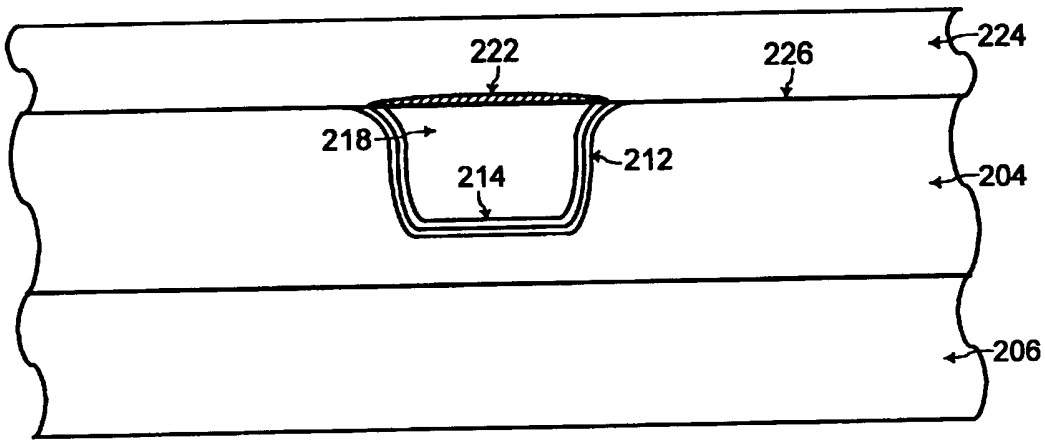
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FIG. 13

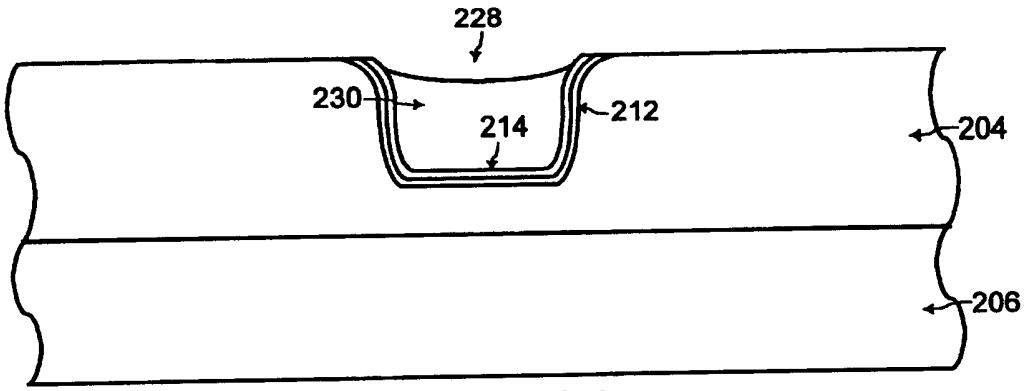

FIG. 14

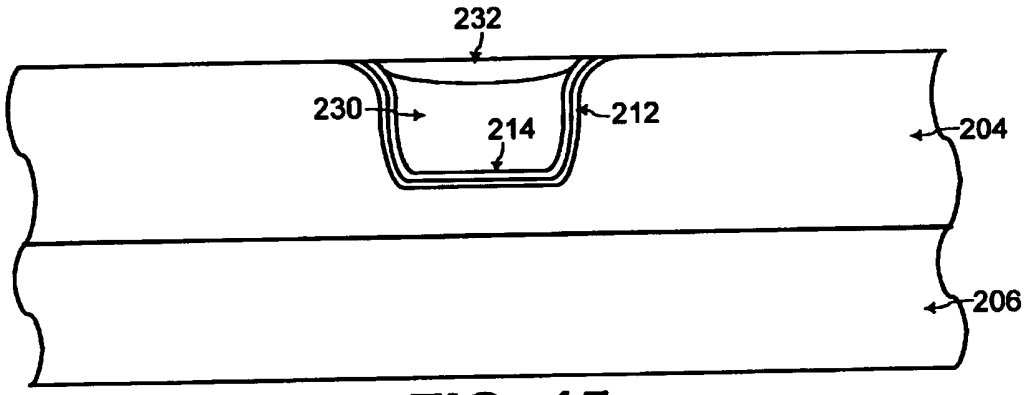

FIG. 15

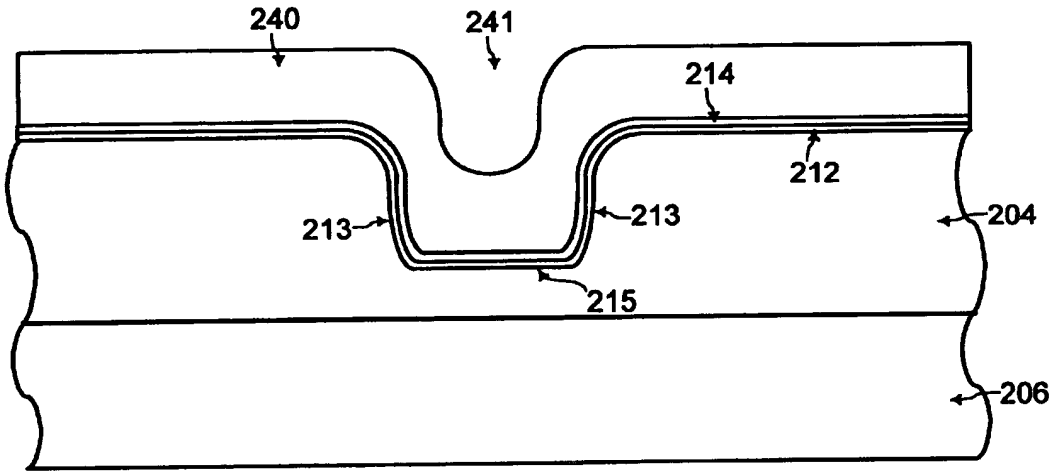
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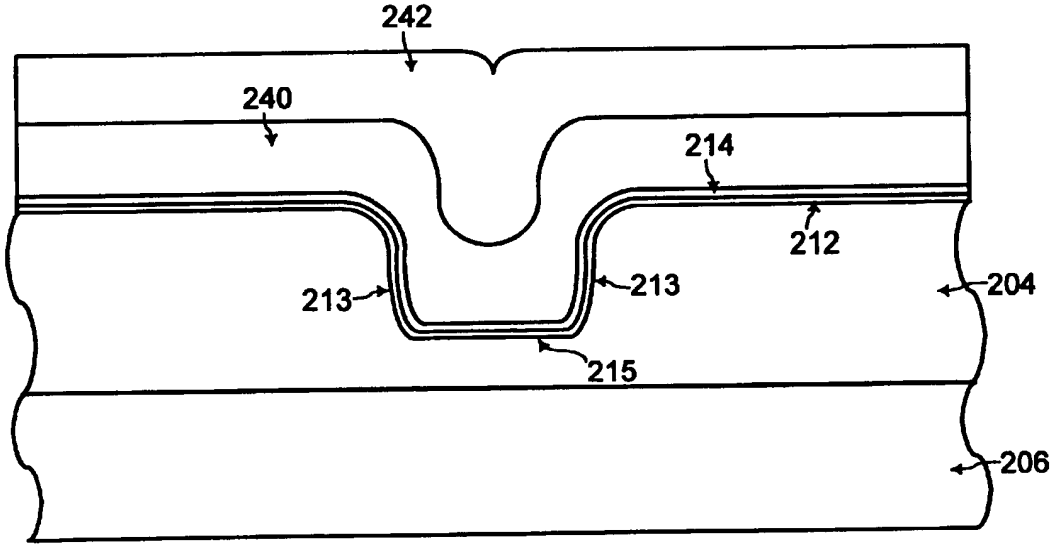
FIG. 16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206

FIG. 17

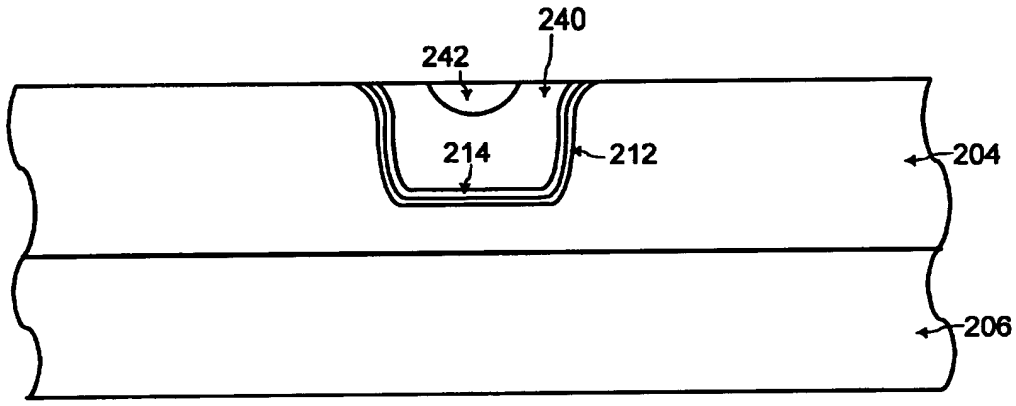

FIG. 18

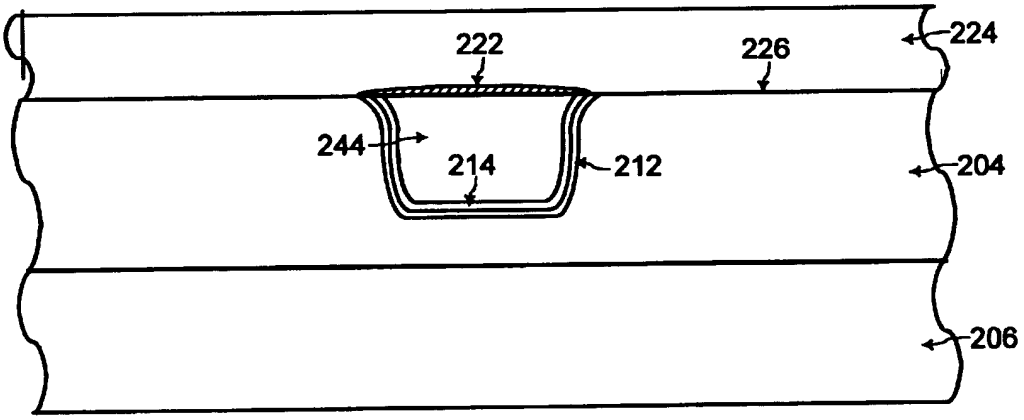

FIG. 19

FILLING AN INTERCONNECT OPENING WITH DIFFERENT TYPES OF ALLOYS TO ENHANCE INTERCONNECT RELIABILITY

TECHNICAL FIELD

The present invention relates generally to fabrication of interconnect, such as copper interconnect for example, within an integrated circuit, and more particularly, to using different types of metal alloys for the seed layer and the conductive fill for filling an interconnect opening to minimize electromigration and void formation within the interconnect.

BACKGROUND OF THE INVENTION

A long-recognized important objective in the constant advancement of monolithic IC (Integrated Circuit) technology is the scaling-down of IC dimensions. Such scaling-down of IC dimensions reduces area capacitance and is critical to obtaining higher speed performance of integrated circuits. Moreover, reducing the area of an IC die leads to higher yield in IC fabrication. Such advantages are a driving force to constantly scale down IC dimensions.

Thus far, aluminum has been prevalently used for metallization within integrated circuits. However, as the width of metal lines are scaled down to smaller submicron and even nanometer dimensions, aluminum metallization shows electromigration failure. Electromigration failure, which may lead to open and extruded metal lines, is now a commonly recognized problem. Moreover, as dimensions of metal lines further decrease, metal line resistance increases substantially, and this increase in line resistance may adversely affect circuit performance.

Given the concerns of electromigration and line resistance with smaller metal lines and vias, copper is considered a more viable metal for smaller metallization dimensions. Copper has lower bulk resistivity and potentially higher electromigration tolerance than aluminum. Both the lower bulk resistivity and the higher electromigration tolerance improve circuit performance.

Referring to FIG. **1**, a cross sectional view is shown of a copper interconnect **102** within a trench **104** formed in an insulating layer **106**. The copper interconnect **102** within the insulating layer **106** is formed on a semiconductor wafer **108** such as a silicon substrate as part of an integrated circuit. Because copper is not a volatile metal, copper cannot be easily etched away in a deposition and etching process as typically used for aluminum metallization. Thus, the copper interconnect **102** is typically formed by etching the trench **104** as an opening within the insulating layer **106**, and the trench **104** is then filled with copper typically by an electroplating process, as known to one of ordinary skill in the art of integrated circuit fabrication.

Unfortunately, copper is a mid-bandgap impurity in silicon and silicon dioxide. Thus, copper may diffuse easily into these common integrated circuit materials. Referring to FIG. **1**, the insulating layer **106** may be comprised of silicon dioxide or a low dielectric constant insulating material such as organic doped silica, as known to one of ordinary skill in the art of integrated circuit fabrication. Copper may easily diffuse into such an insulating layer **106**, and this diffusion of copper may degrade the performance of the integrated circuit. Thus, a diffusion barrier material **110** is deposited to surround the copper interconnect **102** within the insulating layer **106** on the sidewalls and the bottom wall of the copper interconnect **102**, as known to one of ordinary skill in the art of integrated circuit fabrication. The diffusion barrier material **110** is disposed between the copper interconnect **102** and the insulating layer **106** for preventing diffusion of copper from the copper interconnect **102** to the insulating layer **106** to preserve the integrity of the insulating layer **106**.

Further referring to FIG. **1**, an encapsulating layer **112** is deposited as a passivation layer to encapsulate the copper interconnect **102**, as known to one of ordinary skill in the art of integrated circuit fabrication. The encapsulating layer **112** is typically comprised of a dielectric such as silicon nitride, and copper from the copper interconnect **102** does not easily diffuse into such a dielectric of the encapsulating layer **112**.

Referring to FIG. **1**, in the prior art, the encapsulating layer **112** of silicon nitride is deposited directly onto an exposed surface of the copper interconnect **102** and the surrounding insulating layer **106** after the exposed surface of the copper interconnect **102** and the surrounding insulating layer **106** are polished to a level surface. Unfortunately, the silicon nitride of the encapsulating layer **112** does not bond well to the copper at the exposed surface of the copper interconnect **102**.

Thus, although copper does not diffuse easily through the encapsulating layer **112** of silicon nitride, copper from the copper interconnect **102** laterally drifts from the interface between the copper interconnect **102** and the encapsulating layer **112** of silicon nitride along the bottom surface **114** of the encapsulating layer **112** of silicon nitride because of the weak bonding of the copper interconnect **102** and the encapsulating layer **112** of silicon nitride.

The copper that laterally drifts from the interface between the copper interconnect **102** and the encapsulating layer **112** of silicon nitride along the bottom surface **114** of the encapsulating layer **112** eventually diffuses into the insulating layer **106** to disadvantageously degrade the insulating property of the insulating layer **106** and to possibly degrade the copper interconnect electromigration life-time. Nevertheless, use of copper metallization is desirable for further scaling down integrated circuit dimensions because of the lower bulk resistivity and the higher electromigration tolerance. Thus, a mechanism is desired for preventing the drift of copper from the copper interconnect **102** into the insulating layer **106**.

In addition, typically for filling the trench **104** with copper, a seed layer of copper is deposited on the sidewalls and the bottom wall of the trench, and then copper is electroplated from the seed layer to fill the trench **104** in an ECD (electro chemical deposition) process, as known to one of ordinary skill in the art of integrated circuit fabrication. The seed layer of copper is typically deposited by a conformal deposition process such as a PVD (plasma vapor deposition) process or a CVD (chemical vapor deposition) process as known to one of ordinary skill in the art of integrated circuit fabrication. With such conformal deposition processes, referring to FIG. **2**, when the aspect ratio (defined as the depth to the width) of an interconnect opening **120** to be filled with copper is relatively large (i.e., greater than 5:1), a seed layer **122** that is deposited on the sidewalls and the bottom wall of the opening **120** may have a significant overhang **124** at the top corners of the interconnect opening **120**.

Referring to FIGS. **2** and **3**, when copper fill **126** is plated from the seed layer **122**, the copper that is plated from the overhang **124** may close off the top of the interconnect opening **120** before a center portion of the interconnect opening **120** is filled with copper to result in formation of a void **128** within the copper fill **126** toward the center of the interconnect opening **120**. Such a void **128** disadvanta-

geously increases the resistance of the interconnect and may even contribute to electromigration failure of the interconnect.

Referring to FIG. **4**, to minimize the overhang **124** at the top corners of the interconnect opening **120**, the seed layer of copper **122** is deposited to be thinner. However, the deposition of the seed layer **122** is not perfectly conformal with the seed layer **122** being even thinner at the sidewalls of the interconnect opening **120**. With such a thinner seed layer **122**, the thickness of the seed layer **122** may be as small as tens of angstroms at the sidewalls of the interconnect opening **120**, and granules **130** of agglomerated copper may form at the sidewalls of the interconnect opening **120**. Such granules **130** result in a discontinuous seed layer of copper **122**, and when copper is electroplated from such a discontinuous seed layer of copper **122**, voids are more likely to form within the copper filling the interconnect opening **120**.

Nevertheless, a relatively thin seed layer **122** of copper is desired for minimizing overhang at the top corners of the interconnect opening having high aspect ratio with submicron and even nanometer dimensions. Thus, a mechanism is desired for minimizing formation of granules **130** of agglomerated copper at the sidewalls of the interconnect opening **120** when the seed layer **122** is relatively thin.

SUMMARY OF THE INVENTION

Accordingly, in a general aspect of the present invention, a first type of copper alloy is used for formation of the seed layer of copper to minimize formation of the granules of agglomerated copper at the sidewalls of the interconnect opening. In addition, a second type of copper alloy is used to fill the interconnect opening to form an additional encapsulating material at the top surface of the conductive fill of the interconnect opening to prevent drift of copper from the copper interconnect into the surrounding insulating layer.

In one aspect of the present invention, an interconnect opening of an integrated circuit is filled with a conductive fill with the interconnect opening being within an insulating layer on a semiconductor wafer. A seed layer of a first alloy is deposited conformally onto sidewalls and a bottom wall of the interconnect opening. The first alloy is comprised of a first metal dopant in a bulk conductive material. The first metal dopant has a solid solubility in the bulk conductive material that is higher than about 0.09 atomic percent at about room temperature, and the first metal dopant has a concentration in the bulk conductive material of the seed layer that is lower than the solid solubility of the first metal dopant in the bulk conductive material.

The interconnect opening is filled with the bulk conductive material by growing the bulk conductive material from the seed layer to form a conductive fill within the interconnect opening. At least a portion of the conductive fill is comprised of a second alloy with a second metal dopant having a solid solubility in the bulk conductive material that is less than about 0.1 atomic percent at about room temperature, and the second metal dopant has a concentration in the conductive fill that is higher than the solid solubility of the second metal dopant in the bulk conductive material.

Any of the seed layer of the first alloy and the bulk conductive material are polished away from the insulating layer surrounding the interconnect opening such that the conductive fill is contained within the interconnect opening. A thermal anneal is performed to form an additional encapsulating material that covers a top surface of the conductive fill, and the additional encapsulating material is formed from the second metal dopant diffusing out of the conductive fill during the thermal anneal. A layer of bulk passivation material is formed over the additional encapsulating material and the insulating layer.

Use of the first alloy of the seed layer prevents agglomeration of the bulk conductive material of the seed layer at the sidewalls of the interconnect opening. In addition, because the first metal dopant has a relatively high solid solubility, the first metal dopant remains within the seed layer during the thermal anneal. On the other hand, because the second metal dopant has a relatively low solid solubility within the second alloy of the conductive fill, the second metal dopant diffuses out to the top surface of the conductive fill during the thermal anneal to form the additional encapsulating material for preventing drift of material from the conductive fill along the bottom surface of the layer of bulk passivation material and into the surrounding insulating layer.

The present invention may be used to particular advantage when the bulk conductive material is copper, and when the first metal dopant of the first alloy of the copper seed layer is one of silver and zinc. When the bulk conductive material is copper, the second metal dopant of the second alloy of the conductive fill may be one of tantalum, calcium, and cerium. In that case, the additional encapsulating material may be the second metal dopant. Alternatively, when the second metal dopant of the second alloy of the conductive fill is zirconium, the additional encapsulating material may be an intermetallic compound formed from a reaction of the second metal dopant with copper of the conductive fill during the thermal anneal. When the top surface of the conductive fill is exposed to oxygen plasma during the thermal anneal, the additional encapsulating material may be metal oxide formed from a reaction of the oxygen plasma with the second metal dopant during the thermal anneal.

These and other features and advantages of the present invention will be better understood by considering the following detailed description of the invention which is presented with the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows a cross-sectional view of a copper interconnect formed by copper filling a trench within an insulating layer, according to the prior art;

FIG. **2** shows a cross-sectional view of a seed layer of copper deposited on the sidewalls and bottom wall of an interconnect opening for illustrating the formation of an overhang of the seed layer at the top corners of the interconnect opening when a relatively thick seed layer is deposited, according to the prior art;

FIG. **3** shows a cross-sectional view of a copper fill plated from the seed layer of FIG. **2** for illustrating the formation of a void within the copper fill from the overhang of the seed layer of FIG. **2**, according to the prior art;

FIG. **4** shows a cross-sectional view of a relatively thin seed layer of copper deposited on the sidewalls and bottom wall of an interconnect opening for illustrating the formation of granules of agglomerated copper at the sidewalls of the interconnect opening, according to the prior art; and

FIGS. **5**, **6**, **7**, **8**, **9**, **10**, **11**, **12**, **13**, **14** **15**, **16**, **17**, **18**, and **19** show cross-sectional views for formation of an interconnect to illustrate process steps for forming a conductive fill within an interconnect opening that is formed in an insulating layer by using a first type of copper alloy for the seed layer of copper to minimize formation of granules of

agglomerated copper at the sidewalls of the interconnect opening. In addition, these figures illustrate process steps for using a second type of copper alloy to fill the interconnect opening to form an additional encapsulating material at the top surface of the conductive fill of the interconnect opening to prevent drift of copper from the copper interconnect into the surrounding insulating layer.

The figures referred to herein are drawn for clarity of illustration and are not necessarily drawn to scale. Elements having the same reference number in FIGS. **1**, **2**, **3**, **4**, **5**, **6**, **7**, **8**, **9**, **10**, **11**, **12**, **13**, **14**, **15**, **16**, **17**, **18**, and **19** refer to elements having similar structure and function.

DETAILED DESCRIPTION

The present invention is described for formation of copper interconnect. However, the present invention may be practiced for preventing drift of material from other types of interconnects into the surrounding insulating layer, as would be apparent to one of ordinary skill in the art of integrated circuit fabrication from the description herein.

Referring to FIG. **5**, for forming an interconnect such as copper interconnect, an interconnect opening **202** such as a trench line is formed within an insulating layer **204** on a semiconductor wafer **206** as part of an integrated circuit, as known to one of ordinary skill in the art of integrated circuit fabrication. Typically, the semiconductor wafer **206** is comprised of silicon (Si), and the insulating layer **204** is comprised of silicon dioxide (SiO_2) or a low dielectric constant insulating material such as organic doped silica, as known to one of ordinary skill in the art of integrated circuit fabrication.

Copper interconnect is desirable for metallization within an integrated circuit with scaled down dimensions because copper has lower bulk resistivity and potentially higher electromigration tolerance than aluminum. However, because copper is not a volatile metal, copper cannot be easily etched away in a deposition and etching process as typically used for aluminum metallization. Thus, copper interconnect is typically formed by etching the interconnect opening **202** within the insulating layer **204** and then filling the interconnect opening **202** with copper fill.

Referring to FIG. **6**, the top corners **210** of the interconnect opening **202** are rounded by a sputtering process. Sputtering processes are known to one of ordinary skill in the art of integrated circuit fabrication.

Referring to FIG. **7**, a diffusion barrier layer **212** is deposited on the exposed surfaces of the insulating layer **204** including the sidewalls **213** and the bottom wall **215** of the interconnect opening **202**. The diffusion barrier layer **212** is comprised of a diffusion barrier material that prevents diffusion of copper to be filled within the interconnect opening **202** into the surrounding insulating layer **204**. Such diffusion barrier materials and processes for deposition of such diffusion barrier materials are known to one of ordinary skill in the art of integrated circuit fabrication.

Unfortunately, copper is a mid-bandgap impurity in silicon and silicon dioxide. Thus, copper may diffuse easily into these common integrated circuit materials. Referring to FIG. **2**, the insulating layer **204** is typically comprised of silicon dioxide or a low dielectric constant insulating material such as organic doped silica, as known to one of ordinary skill in the art of integrated circuit fabrication, especially when the semiconductor wafer **206** is a silicon substrate.

Copper may easily diffuse into the insulating layer **204**, and this diffusion of copper may degrade the performance of the integrated circuit. Thus, the diffusion barrier layer **212** is deposited to surround the copper to be filled within the interconnect opening **202**. The diffusion barrier layer **212** prevents diffusion of copper to filled within the interconnect opening **202** to the insulating layer **204** to preserve the integrity of the insulating layer **204**.

Referring to FIG. **8**, a copper seed layer **214** of a first alloy is conformally deposited on the diffusion barrier layer **212**. The first alloy of the copper seed layer **214** is comprised of a first metal dopant that has a relatively high solid solubility (greater than about 0.09 atomic percent at about room temperature) within copper as the bulk conductive material. Examples of such a first metal dopant include silver and zinc. For example, silver has a solid solubility in copper of about 0.1 atomic percent at about room temperature, and zinc has a solid solubility in copper of about 33 atomic percent at about room temperature.

In addition, the first metal dopant has a concentration in copper of the seed layer **214** that is less than the solid solubility of the first metal dopant in copper. For example, when the first metal dopant is silver, the concentration of silver in copper of the seed layer **214** may be in a range of from about 0.01 atomic percent to about 0.09 atomic percent. When the first metal dopant is zinc, the concentration of zinc in copper of the seed layer **214** may be in a range of from about 0.01 atomic percent to about 5.0 atomic percent.

With use of such a copper alloy for the seed layer **214**, the thickness of the seed layer **214** may be relatively thin in a range of from about 20 Å (angstroms) to about 50 Å (angstroms) without formation of granules of agglomerated copper at the sidewalls **213** of the interconnect opening **202**. In contrast, the thickness of a seed layer of pure copper may have a lower limit of about 80 Å (angstroms) before the seed layer agglomerates at the sidewalls **213** of the interconnect opening **202**. In addition, the thickness of a seed layer of pure copper which is more dependent on thermal processes and the type of diffusion barrier layer **212** is harder to control.

The first metal dopant within the copper of the seed layer **214** promotes uniform deposition for a thin continuous seed layer **214** without formation of granules of agglomerated copper at the sidewalls **213** of the interconnect opening **202**. Processes for conformal deposition of such an alloy for the seed layer **214**, such as CVD (chemical vapor deposition), IMP (ionized metal plasma) deposition, and continuous PVD (physical vapor deposition), are known to one of ordinary skill in the art of integrated circuit fabrication.

Referring to FIG. **9**, the interconnect opening **202** is filled with the bulk conductive material **216** of the seed layer **214** by electroplating from the seed layer **214**. Electroplating processes for filling the interconnect opening **202** with the conductive material **216** are known to one of ordinary skill in the art of integrated circuit fabrication.

In one embodiment of the present invention, the whole portion of the conductive material **216** electroplated from the seed layer **214** is comprised of a second alloy with a second metal dopant that has a relatively low solid solubility (less than about 0.1 atomic percent at about room temperature) within copper as the bulk conductive material. Examples of such a second metal dopant include tantalum, calcium, cerium, and zirconium. In addition, the second metal dopant has a concentration in the bulk conductive material **216** that is greater than the solid solubility of the second metal dopant in the bulk conductive material **216**. For example, when the second metal dopant is comprised of one tantalum, calcium, cerium, and zirconium, the concentration of the second metal dopant in the bulk conductive

material **216** comprised of copper may be in a range of from about 0.01 atomic percent to about 1 atomic percent because the solid solubility of such metal dopants is negligible in copper.

Referring to FIG. **10**, any bulk conductive material **216** is polished away from the insulating layer **204** typically using a CMP (Chemical Mechanical Polishing) process such that the bulk conductive material **216** is contained within the interconnect opening **202** to form a conductive fill **218** within the interconnect opening **202**. In addition, the seed layer **214** and the diffusion barrier layer **212** are also typically polished away from the insulating layer **204** during this CMP process to expose the insulating layer **204**. CMP (Chemical Mechanical Polishing) processes are known to one of ordinary skill in the art of integrated circuit fabrication.

Typically, a pre-CMP anneal is performed to ensure consistency of density of copper of the bulk conductive material **216** across the semiconductor wafer **206** before such a polishing process, as known to one of ordinary skill in the art of integrated circuit fabrication. The pre-CMP anneal is typically performed at a temperature in a range of from about 100° Celsius to about 300° Celsius for a time period of from about 30 second to about 60 minutes, as known to one of ordinary skill in the art of integrated circuit fabrication. A shorter anneal time is used for a higher anneal temperature. For example, when the anneal temperature is about 100° Celsius, the anneal time is about 60 minutes, and when the anneal temperature is about 300° Celsius, the anneal time is about 30 seconds. In addition, the anneal temperature and the anneal time depend on the dimensions of the interconnect with a lower anneal temperature and a longer anneal time being used for smaller dimensions of the interconnect.

Such a pre-CMP anneal results in consistency of density of copper of the bulk conductive material **216** across the semiconductor wafer **206** before the polishing process. The metal dopants within the seed layer **214** and the bulk conductive material **216** remain within the seed layer **214** and the bulk conductive material **216** during this pre-CMP anneal process. Such pre-CMP anneal processes are known to one of ordinary skill in the art of integrated circuit fabrication.

Referring to FIGS. **10** and **11**, with the top surface **220** of the conductive fill **218** exposed, a thermal anneal is performed by heating up the semiconductor wafer **206** to a temperature in a range of from about 250° Celsius to about 400° Celsius for a time period in a range of from about 1 minute to about 60 minutes. A shorter anneal time is used for a higher anneal temperature. For example, when the anneal temperature is about 250° Celsius, the anneal time is about 60 minutes, and when the anneal temperature is about 400° Celsius, the anneal time is about 1 minute. Thermal anneal processes are known to one of ordinary skill in the art of integrated circuit fabrication.

During this thermal anneal process, the copper of the conductive fill 218 recrystallizes into a single grain structure of substantially pure copper as the second metal dopant of the conductive fill **218** diffuses out from the conductive fill **218** to the top surface **220** of the conductive fill **218**. The single grain structure of substantially pure copper of the conductive fill **218** minimizes resistance of the interconnect such that the speed performance of the integrated circuit having the interconnect of the present invention is enhanced.

Because the metal dopant has a concentration within the conductive fill **218** that is larger than the solid solubility of the metal dopant in the bulk conductive material of the conductive fill **218**, the metal dopant segregates out of the conductive fill **218** during the thermal anneal. The metal dopant of the conductive fill **218** that segregates out of the conductive fill **218** to the top surface **220** of the conductive fill **218** forms an additional encapsulating material **222** that covers the top surface of the conductive fill **218**.

For example, when the metal dopant of the conductive fill **218** is comprised of one of tantalum, calcium, or cerium, the additional encapsulating material **222** that covers the top surface of the conductive fill **218** is the metal dopant that accumulates at the top surface **220** of the conductive fill **218**. In that case, the additional encapsulating material may also form at the interface between the seed layer **214** and the conductive fill **218**.

Alternatively, when the metal dopant of the conductive fill **218** is comprised of zirconium for example, the additional encapsulating material **222** that covers the top surface of the conductive fill **218** is an intermetallic compound formed from a reaction of the metal dopant with the copper at the top surface of the conductive fill **218**. Referring to FIG. **12**, in an alternative embodiment of the present invention, the top surface of the conductive fill **218** is exposed to oxygen plasma during the thermal anneal. In that case, when the metal dopant of the conductive fill **218** is comprised of zirconium for example, the additional encapsulating material **222** that covers the top surface of the conductive fill **218** is a metal oxide formed from a reaction of the metal dopant with the oxygen plasma at the top surface of the conductive fill **218**. Processes for formation of oxygen plasma are known to one of ordinary skill in the art of integrated circuit fabrication.

Referring to FIG. **13**, for any type of the additional encapsulating material **222**, a layer of bulk passivation material **224** is deposited on the additional encapsulating material **222** and the insulating layer **204**. The bulk passivation material **224** may be comprised of one of silicon oxynitride (SiON), silicon nitride (SiN), and a silicon carbide (SiC) film doped with hydrogen, and copper does not easily diffuse through such a bulk passivation material **224**. Processes for depositing such bulk passivation material **224** are known to one of ordinary skill in the art of integrated circuit fabrication.

In this manner, the additional encapsulating material **222** which covers the top surface of the conductive fill **218** prevents copper of the conductive fill **218** from laterally drifting along the bottom surface **226** of the layer of bulk passivation material **224** and into the surrounding insulating layer **204**. The additional encapsulating material **222** caps the conductive fill **218** such that the copper of the conductive fill **218** is contained within the trench **202**. Minimization of drift of copper from the conductive fill **218** into the surrounding insulating layer **204** preserves the integrity of the surrounding insulating layer **204**.

In addition, because the metal dopant has a concentration in the seed layer **214** that is lower than the solid solubility of the metal dopant in the bulk conductive material of the seed layer **214**, the metal dopant of the seed layer **214** remains within the seed layer **214** during the thermal anneal for recrystallizing the conductive fill **218**. The alloy of the seed layer **214** is used primarily to prevent formation of granules of agglomerated copper during conformal deposition of the seed layer **214** on the sidewalls and the bottom wall of the interconnect opening **202**. In addition, the metal dopant, such as silver or zinc, of the copper seed layer **214** minimally increases the resistance of the copper seed layer **214**.

For example, when the metal dopant of the copper seed layer **214** is silver, the increase in resistance for such a copper alloy is about 0.2 microOhms-centimeters per 1 atomic percent silver doping concentration. When the metal dopant of the copper seed layer **214** is zinc, the increase in resistance for such a copper alloy is about 0.3 microOhms-centimeters per 1 atomic percent zinc doping concentration. Such increase in resistance is smaller than other types of metal dopants of copper alloys.

Referring to FIGS. **14** and **15**, in an alternative embodiment of the present invention, a portion of the conductive material filling the interconnect opening may be comprised of an alloy. In that case, referring to FIG. **9**, the bulk conductive material **216** deposited to fill the interconnect opening **202** is comprised of substantially pure copper. Referring to FIGS. **9** and **14**, the bulk conductive material **216** of substantially pure copper is polished down to form a recess **228** during the CMP (chemical mechanical polishing) process. In that case, a substantially pure copper fill **230** is contained at the bottom portion of the interconnect opening **202**.

The recess **228** is formed on the top surface of the substantially pure copper fill **230** according to the "dishing effect" during a CMP process, as known to one of ordinary skill in the art of integrated circuit fabrication. Parameters of the CMP process such as the roughness of the polishing pad may be controlled to affect the formation of the recess **228** on the top surface of the substantially pure copper fill **230**, as known to one of ordinary skill in the art of integrated circuit fabrication. Typically, the "dishing effect" and the formation of a recess on an interconnect are avoided in the prior art, but in an aspect of the present invention, parameters of the CMP are intentionally controlled for formation of the recess **228** on the top surface of the substantially pure copper fill **230**.

Referring to FIGS. **14** and **15**, a second copper alloy **232** with the second metal dopant is deposited to fill the recess **228** at the top portion of the interconnect opening. As described for the copper alloy of the conductive fill **218** of FIGS. **10**, **11**, **12**, and **13**, the second metal dopant has a relatively low solid solubility (less than about 0.1 atomic percent at about room temperature) within the copper of the second copper alloy **232**. Examples of such a second metal dopant include tantalum, calcium, cerium, and zirconium. In addition, the second metal dopant has a concentration in the copper of the second copper alloy **232** that is greater than the solid solubility of the second metal dopant in copper. For example, when the second metal dopant is comprised of one tantalum, calcium, cerium, or zirconium, the concentration of the second metal dopant in the bulk conductive material **216** comprised of copper may be in a range of from about 0.1 atomic percent to about 1 atomic percent because the solid solubility of such metal dopants in copper is negligible.

With such a copper alloy **232** at the top portion of the interconnect opening, during the thermal anneal for recrystallizing the substantially pure copper fill **230** and the second copper alloy **232**, the substantially pure copper fill **230** and the second copper alloy **232** recrystallize to form a conductive fill of a substantially single grain structure within the interconnect opening **202**. In addition, during the thermal anneal, the metal dopant of the copper alloy **232** segregates out of the copper alloy **232** to the top surface **220** of the conductive fill to form the additional encapsulating material **222** that covers the top surface of the conductive fill, similarly as described in relation to FIGS. **11** and **12** to prevent drift of conductive material from the conductive fill of the interconnect opening **202** into the surrounding insulating layer **204**.

In another embodiment of the present invention, referring to FIG. **16**, a layer of substantially pure copper **240** is deposited in the interconnect opening **202**. The layer of substantially pure copper **240** is typically electroplated from the seed layer **214**, as known to one of ordinary skill in the art of integrated circuit fabrication. The layer of substantially pure copper **240** is deposited to only partially fill the interconnect opening **202** (i.e., about 70% to 90% of the volume of the interconnect opening **202**) to leave a recess **241** within the layer of substantially pure copper **240**. The recess **241** is disposed toward the top of the interconnect opening **202**.

Referring to FIG. **17**, the recess **241** is filled with a second copper alloy **242** with a second metal dopant. As described for the copper alloy of the conductive fill **218** of FIGS. **10**, **11**, **12**, and **13**, the second metal dopant has a relatively low solid solubility (less than about 0.1 atomic percent at about room temperature) within the copper of the second copper alloy **242**. Examples of such a second metal dopant include tantalum, calcium, cerium, and zirconium. In addition, the second metal dopant has a concentration in the copper of the second copper alloy **242** that is greater than the solid solubility of the second metal dopant in copper. For example, when the second metal dopant is comprised of one tantalum, calcium, cerium, or zirconium, the concentration of the second metal dopant in the bulk conductive material comprised of copper may be in a range of from about 0.1 atomic percent to about 1 atomic percent because the solid solubility of such metal dopants in copper is negligible. Processes such as PVD (plasma vapor deposition) and CVD (chemical vapor deposition) for depositing such a second copper alloy **242** in the recess **241** are known to one of ordinary skill in the art of integrated circuit fabrication.

Referring to FIG. **18**, the layer of substantially pure copper **240** and the second copper alloy **242** are polished away from the insulating layer **204** until the insulating layer **204** is exposed such that the substantially pure copper **240** and the second copper alloy **242** are contained within the interconnect opening **202**. In this manner, the second copper alloy **242** is formed at the top of the interconnect opening **202**. Processes such as CMP (chemical mechanical polishing) processes for polishing away the layer of substantially pure copper **240** and the second copper alloy **242** are known to one of ordinary skill in the art of integrated circuit fabrication.

Referring to FIGS. **18** and **19**, with the second copper alloy **242** at the top portion of the interconnect opening, during the thermal anneal for recrystallizing the substantially pure copper **240** and the second copper alloy **242**, the substantially pure copper **240** and the second copper alloy **242** recrystallize to form a conductive fill of a substantially single grain structure **244** within the interconnect opening. In addition, during the thermal anneal, the metal dopant of the copper alloy **242** segregates out of the copper alloy **242** to the top surface of the conductive fill **244** to form the additional encapsulating material **222** that covers the top surface of the conductive fill, similarly as described in relation to FIGS. **11** and **12**. The additional encapsulating material **222** prevents drift of conductive material from the conductive fill **244** of the interconnect opening along the bottom surface **226** of the layer of bulk passivation material **224** and into the surrounding insulating layer **204**.

The foregoing is by way of example only and is not intended to be limiting. For example, the present invention is described for formation of copper interconnect. However, the present invention may be practiced for preventing drift of material from other types of interconnects into the sur-

rounding insulating layer, as would be apparent to one of ordinary skill in the art of integrated circuit fabrication from the description herein. Any material specified herein is by way of example only.

Furthermore, as will be understood by those skilled in the art, the structures described herein may be made or used in the same way regardless of their position and orientation. Accordingly, it is to be understood that terms and phrases such as "top," "bottom," and "sidewalls" as used herein refer to relative location and orientation of various portions of the structures with respect to one another, and are not intended to suggest that any particular absolute orientation with respect to external objects is necessary or required. The present invention is limited only as defined in the following claims and equivalents thereof.

We claim:

1. A method for filling an interconnect opening of an integrated circuit, said interconnect opening being within an insulating layer on a semiconductor wafer, the method including the steps of:

A. depositing a seed layer of a first alloy conformally onto sidewalls and a bottom wall of said interconnect opening, wherein said first alloy is comprised of a first metal dopant in a bulk conductive material, and wherein said first metal dopant has a solid solubility in said bulk conductive material that is higher than about 0.09 atomic percent at about room temperature, and wherein said first metal dopant has a concentration in said bulk conductive material of said seed layer that is lower than said solid solubility of said first metal dopant in said bulk conductive material;

B. filling said interconnect opening with said bulk conductive material by growing said bulk conductive material from said seed layer to form a conductive fill within said interconnect opening, wherein at least a portion of said conductive fill is comprised of a second alloy with a second metal dopant having a solid solubility in said bulk conductive material that is less than about 0.1 atomic percent at about room temperature, and wherein said second metal dopant has a concentration in said portion of said conductive fill that is higher than said solid solubility of said second metal dopant in said bulk conductive material;

C. polishing away any of said seed layer of said first alloy and said bulk conductive material from said insulating layer surrounding said interconnect opening such that said conductive fill is contained within said interconnect opening and such that said insulating layer surrounding said interconnect opening is exposed;

D. performing a thermal anneal after said step C to form an additional encapsulating material that covers a top surface of said conductive fill contained within said interconnect opening with said insulating layer surrounding said interconnect opening being exposed, wherein said additional encapsulating material is formed from said second metal dopant diffusing out of said conductive fill during said thermal anneal; and

E. forming a layer of bulk passivation material over said additional encapsulating material and said insulating layer.

2. The method of claim 1, wherein said bulk conductive material is copper, and wherein said first metal dopant is one of silver and zinc.

3. The method of claim 1, wherein said additional encapsulating material is comprised of said second metal dopant that diffuses out of said conductive fill to cover said top surface of said conductive fill during said thermal anneal.

4. The method of claim 3, wherein said bulk conductive material is copper, and wherein said second metal dopant is one of tantalum, calcium, and cerium.

5. The method of claim 3, wherein said additional encapsulating material also forms along an interface between said conductive fill and said seed layer during said thermal anneal.

6. The method of claim 1, wherein said additional encapsulating material is an intermetallic compound formed from a reaction of said second metal dopant with said bulk conductive material at said top surface of said conductive fill during said thermal anneal.

7. The method of claim 6, wherein said bulk conductive material is copper, and wherein said second metal dopant is zirconium.

8. The method of claim 1, further including a step of:

depositing a diffusion barrier material on sidewalls and a bottom wall of said interconnect opening before said step A.

9. The method of claim 1, wherein said bulk encapsulating layer is comprised of one of silicon oxynitride (SiON), silicon nitride (SiN), and a silicon carbide (SiC) film doped with hydrogen.

10. The method of claim 1, wherein said step D of performing said thermal anneal includes heating said semiconductor wafer to a temperature in a range of from about 250° Celsius to about 400° Celsius for a time period in a range of from about 1 minute to about 60 minutes.

11. A method for filling an interconnect opening of an integrated circuit, said interconnect opening being within an insulating layer on a semiconductor wafer, the method including the steps of:

A. depositing a seed layer of a first alloy conformally onto sidewalls and a bottom wall of said interconnect opening, wherein said first alloy is comprised of a first metal dopant in a bulk conductive material, and wherein said first metal dopant has a solid solubility in said bulk conductive material that is higher than about 0.09 atomic percent at about room temperature, and wherein said first metal dopant has a concentration in said bulk conductive material of said seed layer that is lower than said solid solubility of said first metal dopant in said bulk conductive material;

B. filling said interconnect opening with said bulk conductive material by growing said bulk conductive material from said seed layer to form a conductive fill within said interconnect opening, wherein at least a portion of said conductive fill is comprised of a second alloy with a second metal dopant having a solid solubility in said bulk conductive material that is less than about 0.1 atomic percent at about room temperature, and wherein said second metal dopant has a concentration in said portion of said conductive fill that is higher than said solid solubility of said second metal dopant in said bulk conductive material;

C. polishing away any of said seed layer of said first alloy and said bulk conductive material from said insulating layer surrounding said interconnect opening such that said conductive fill is contained within said interconnect opening;

D. performing a thermal anneal to form an additional encapsulating material that covers a top surface of said conductive fill, wherein said additional encapsulating material is formed from said second metal dopant diffusing out of said conductive fill during said thermal anneal;

E. forming a layer of bulk passivation material over said additional encapsulating material and said insulating layer; and

F. exposing said top surface of said conductive fill to an oxygen plasma during said thermal anneal in said step D such that said additional encapsulating material is comprised of a metal oxide formed from a reaction of said oxygen plasma and said second metal dopant during said thermal anneal.

12. The method of claim 11, wherein said bulk conductive material is copper, and wherein said second metal dopant is zirconium.

13. The method of claim 11, wherein said bulk conductive material is copper, and wherein said first metal dopant is one of silver and zinc.

14. The method of claim 11, further including a step of:

depositing a diffusion barrier material on sidewalls and a bottom wall of said interconnect opening before said step A.

15. The method of claim 11, wherein said bulk encapsulating layer is comprised of one of silicon oxynitride (SiON), silicon nitride (SiN), and a silicon carbide (SiC) film doped with hydrogen.

16. The method of claim 11, wherein said step D of performing said thermal anneal includes heating said semiconductor wafer to a temperature in a range of from about 250° Celsius to about 400° Celsius for a time period in a range of from about 1 minute to about 60 minutes.

* * * * *

US006254966B1

(12) **United States Patent**
Kondo

(10) **Patent No.: US 6,254,966 B1**
(45) **Date of Patent: Jul. 3, 2001**

(54) **INFORMATION RECORDING MEDIUMS, SUPPORTER USED IN THE MEDIUMS, MANUFACTURE METHODS OF THE SUPPORTER, MANUFACTURING APPARATUS OF THE SUPPORTER AND STAMPERS FOR PRODUCING THE MEDIUMS**

(75) Inventor: **Tetsuya Kondo**, Kanagawa-ken (JP)

(73) Assignee: **Victor Company of Japan, Ltd.**, Yokohama (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/366,663**

(22) Filed: **Aug. 3, 1999**

(30) **Foreign Application Priority Data**

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Sep. 18, 1998 (JP) 10-264363
Jan. 26, 1999 (JP) 11-016850

(51) **Int. Cl.**[7] **G11B 7/24**
(52) **U.S. Cl.** ..... **428/156**; 428/64.2; 428/64.3; 428/64.4; 428/694 TR; 360/135; 369/277; 369/284; 369/280
(58) **Field of Search** ..... 360/135; 428/156, 428/64.2, 64.3, 64.4, 694 TR; 369/277, 284, 280

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* cited by examiner

Primary Examiner—William P. Watkins, III
(74) *Attorney, Agent, or Firm*—Anderson, Kill & Olick, P.C.

(57) **ABSTRACT**

An information recording medium and a supporter used for the information recording medium capable of recording a land/groove recording by using a high density recording technique such as a super-resolution, resulting in a high density recording. An information recording medium B has a supporter **1A**, on which a recording layer **5** is formed. On the supporter **1A**, lands **2** and groove **3** are alternately formed as a minute track pattern. A crevice **4** having a depth Dc larger than a depth Dg of the respective grooves **3** is formed in the respective grooves **3** at one end of the respective grooves **3** in a width direction of the respective grooves.

14 Claims, 13 Drawing Sheets

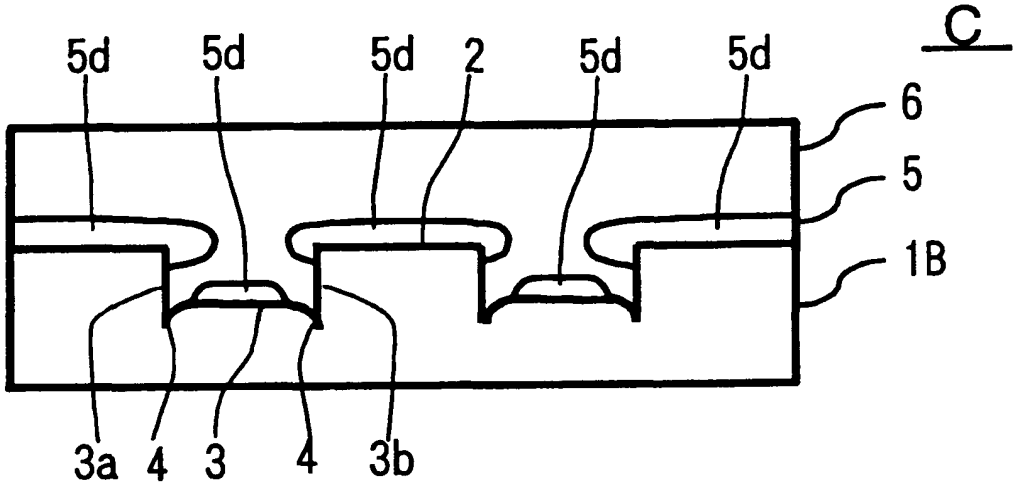


Fig. 1

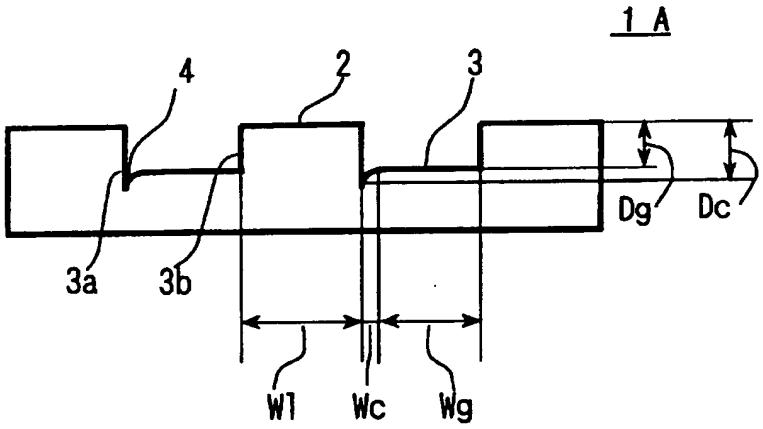


Fig. 2

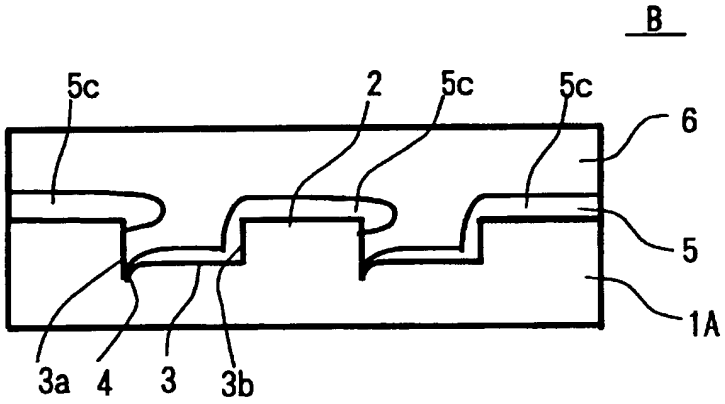


Fig. 3

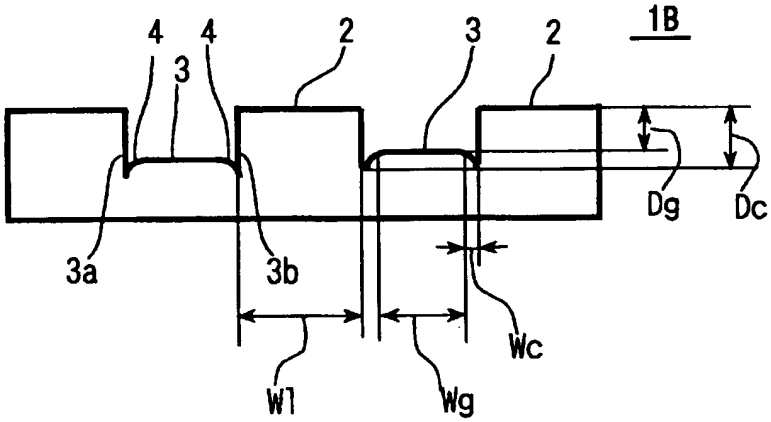


Fig. 4

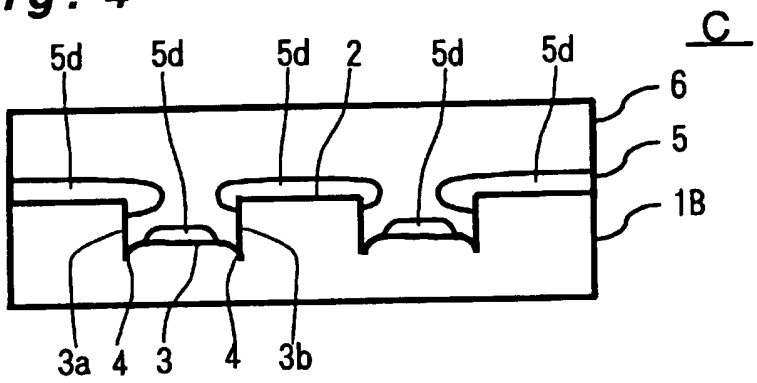


Fig. 5 Prior Art

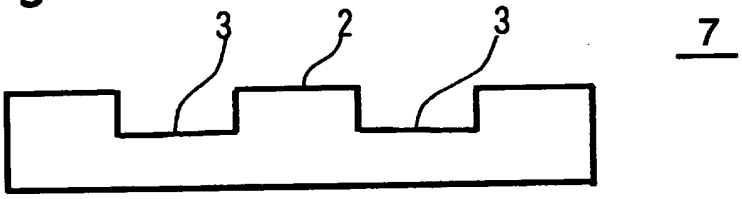


Fig. 6 Prior Art

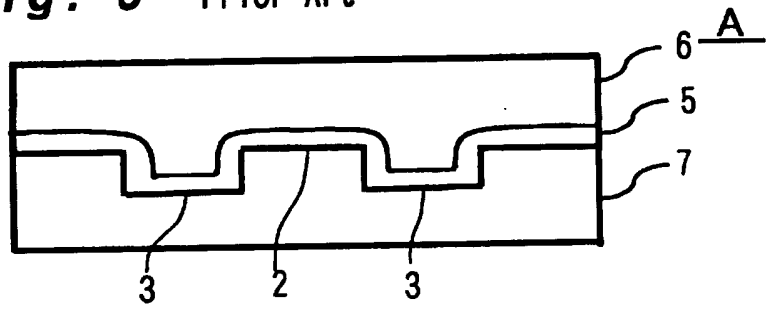


Fig. 7 Prior Art

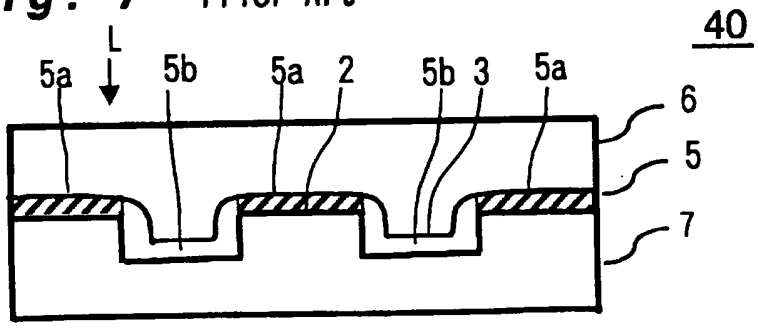


Fig. 8

W1	Wg	Dg	Wc	Dc
0.55 μm	0.51 μm	0.20 μm	0.04 μm	0.35 μm

Fig. 9

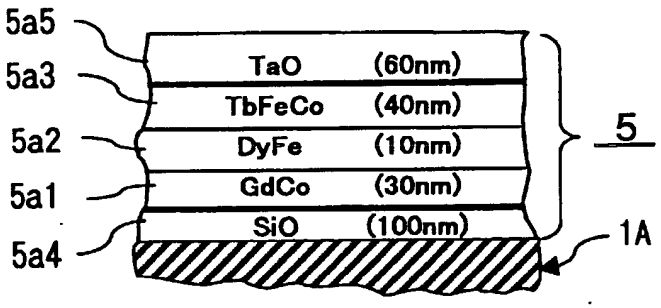


Fig. 10

W1	Wg	Dg	Wc	Dc
0.51 μm	0.51 μm	0.20 μm	0.04 μm	0.35 μm

Fig. 11

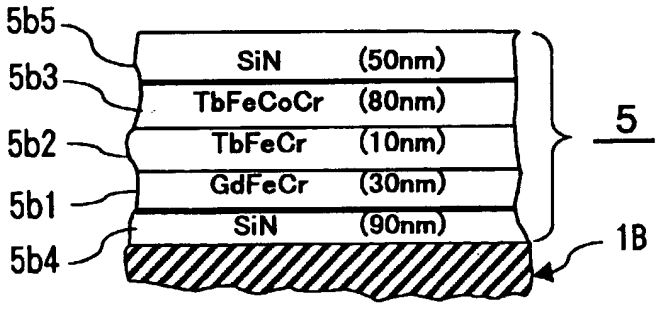


Fig. 12

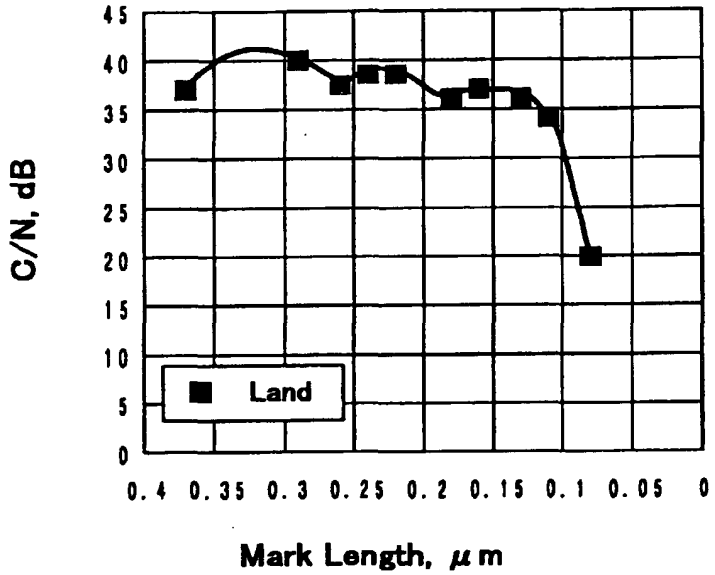

C/N, dB
45
40
35
30
25
20
15
10
5
0
Land
0.4 0.35 0.3 0.25 0.2 0.15 0.1 0.05 0
Mark Length, μm

Fig. 13

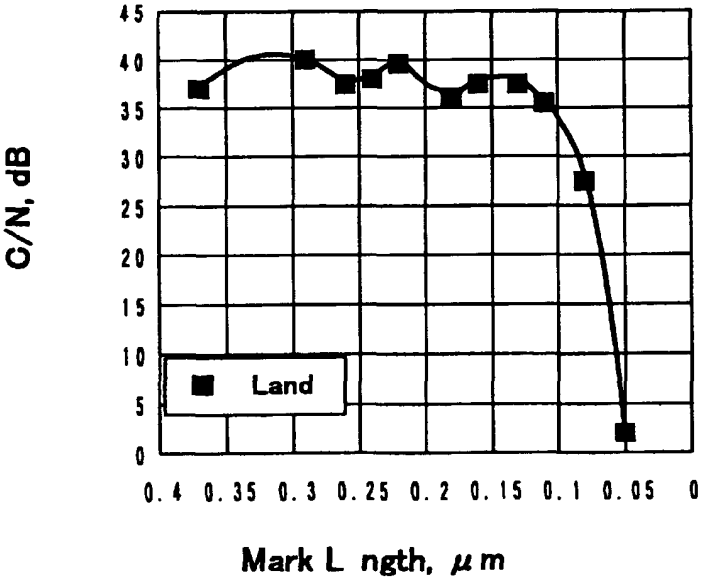

C/N, dB
45
40
35
30
25
20
15
10
5
0
Land
0.4 0.35 0.3 0.25 0.2 0.15 0.1 0.05 0
Mark L ngth, μm

Fig. 14

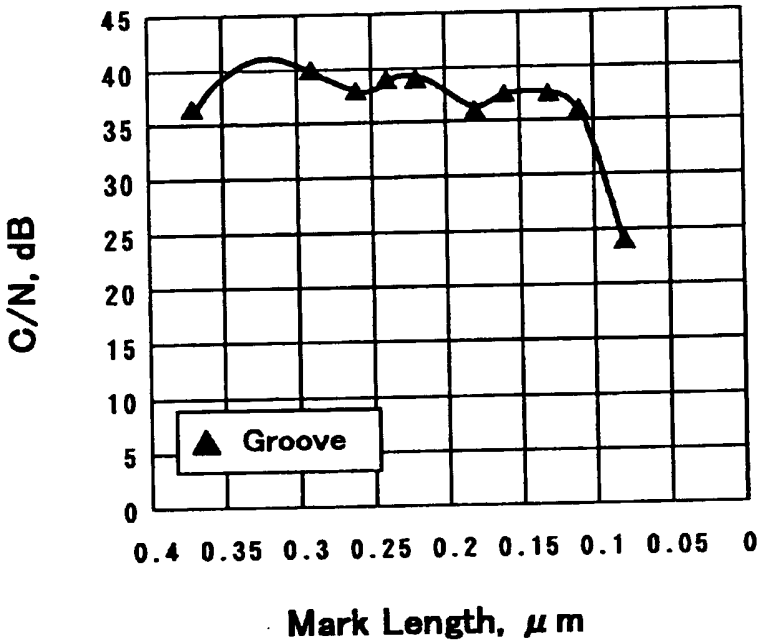

45
40
35
30
25
20
15
10
5
0
C/N, dB
Groove
0.4 0.35 0.3 0.25 0.2 0.15 0.1 0.05 0
Mark Length, μm

Fig. 15 (a)

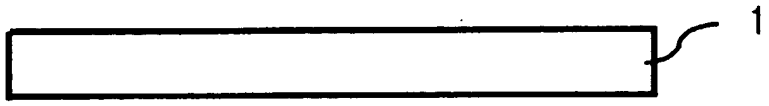


Fig. 15 (b)

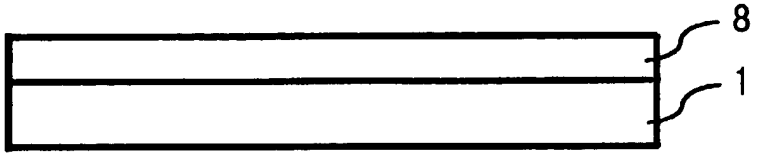


Fig. 15 (c)

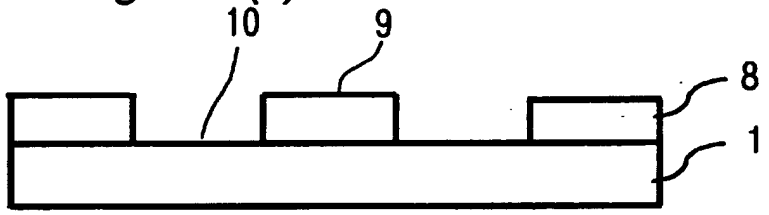


Fig. 15 (d)

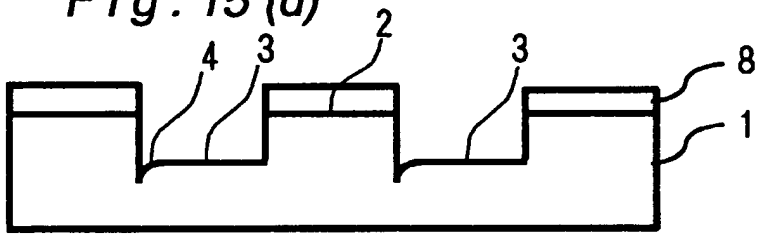


Fig. 15 (e)

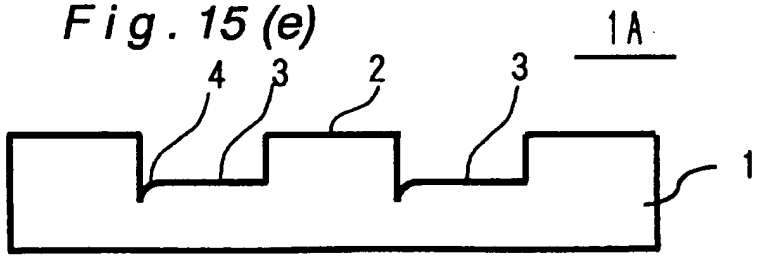


Fig. 16 (a)

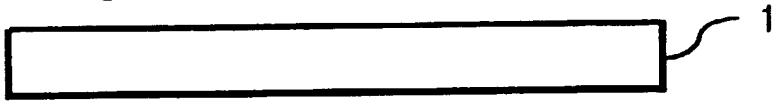


Fig. 16 (b)

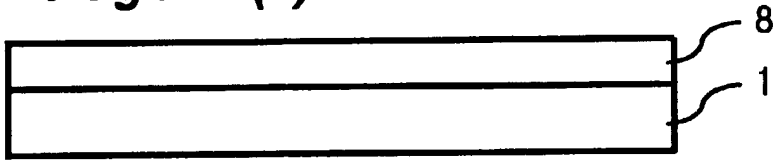


Fig. 16 (c)

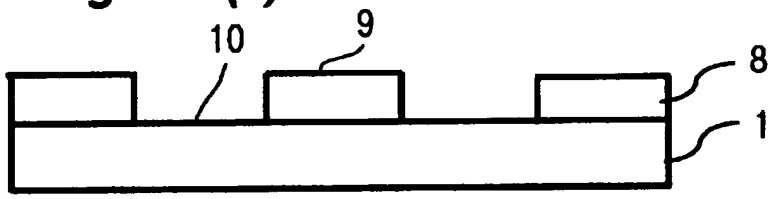


Fig. 16 (d)

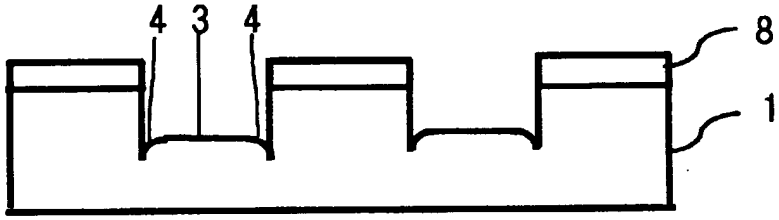


Fig. 16 (e)

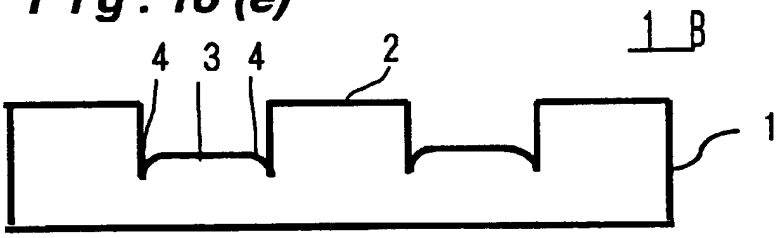
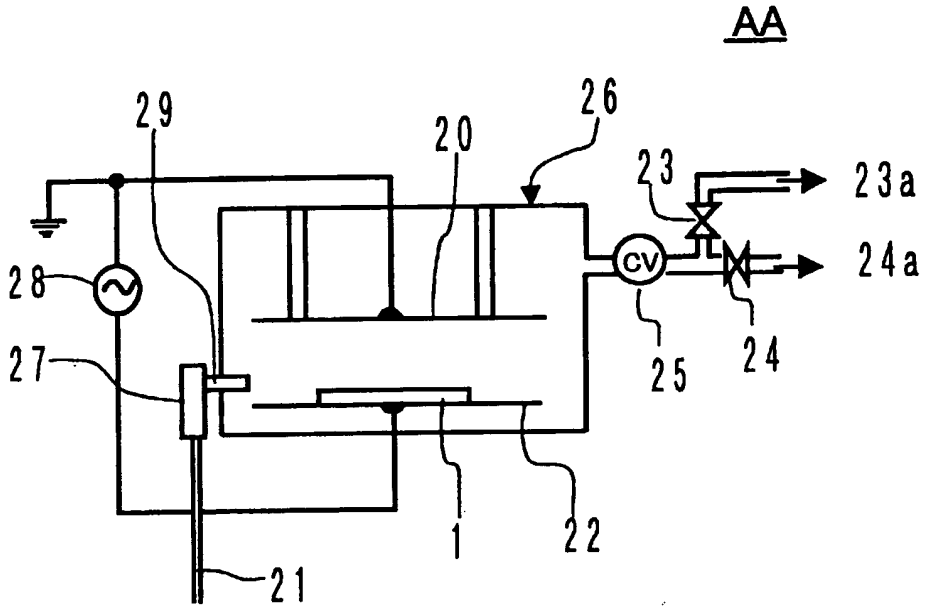


Fig. 17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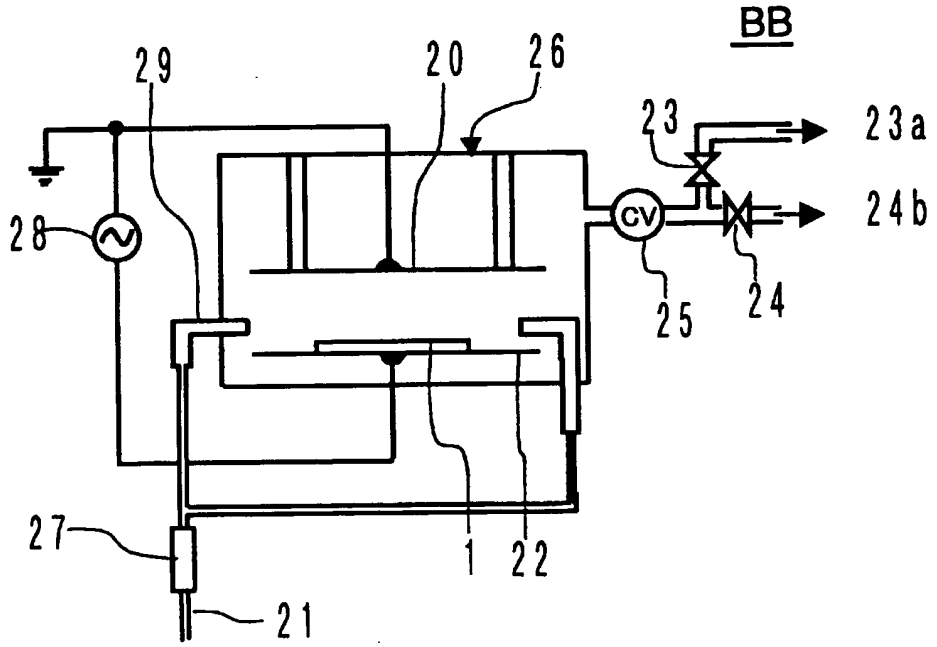
20
26
23
23a
24a
28
CV
27
25
24
1
22
21

Fig. 18


BB
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20
26
23
23a
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CV
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24
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22
21

Fig. 19 (a)

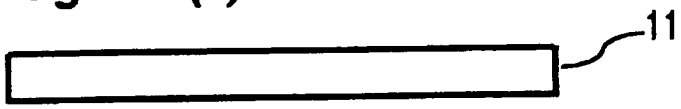


Fig. 19 (b)

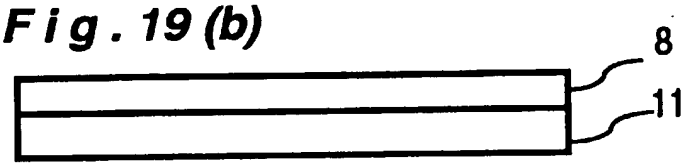


Fig. 19 (c)

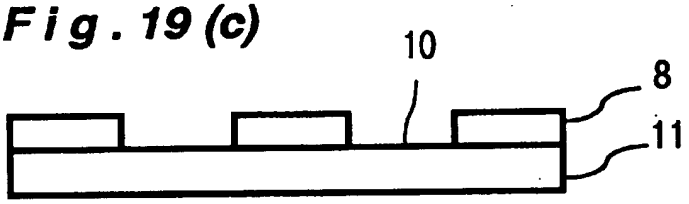


Fig. 19 (d)

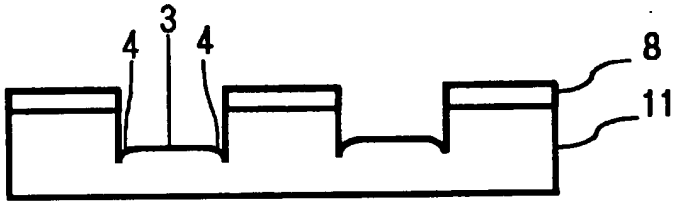


Fig. 19 (e)

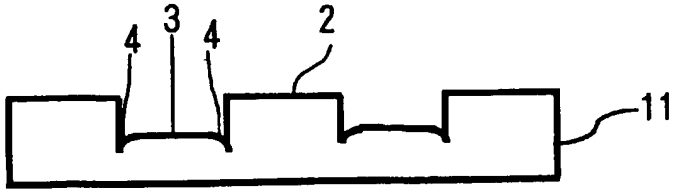


Fig. 19 (f)

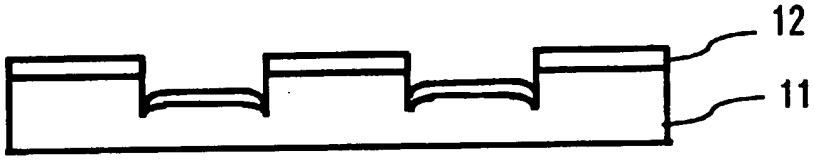


Fig. 19 (g)

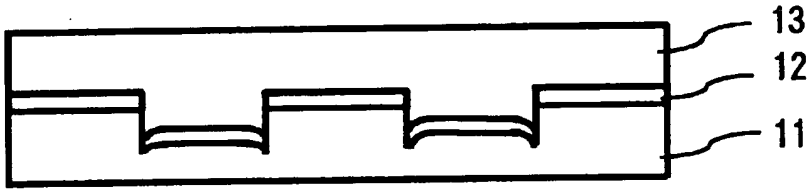


Fig. 19 (h)

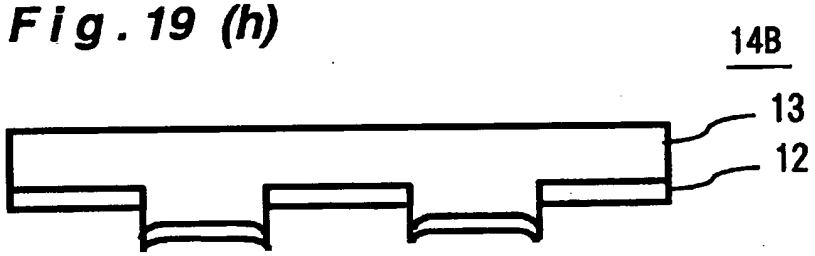


Fig. 19 (i)

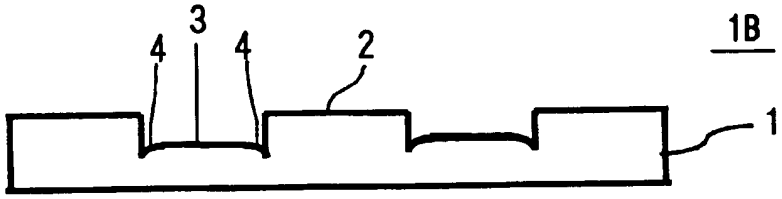
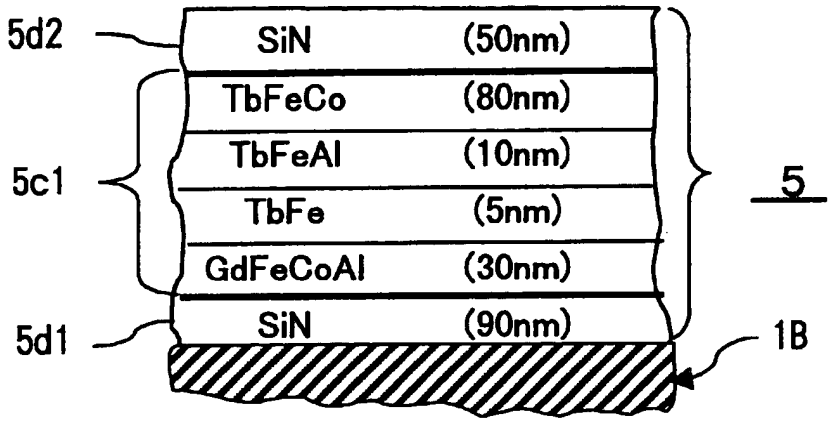


Fig. 20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SiN (50nm)
TbFeCo (80nm)
TbFeAl (10nm)
5c1
TbFe (5nm)
5
GdFeCoAl (30nm)
SiN (90nm)
5d1
1B

Fig. 21

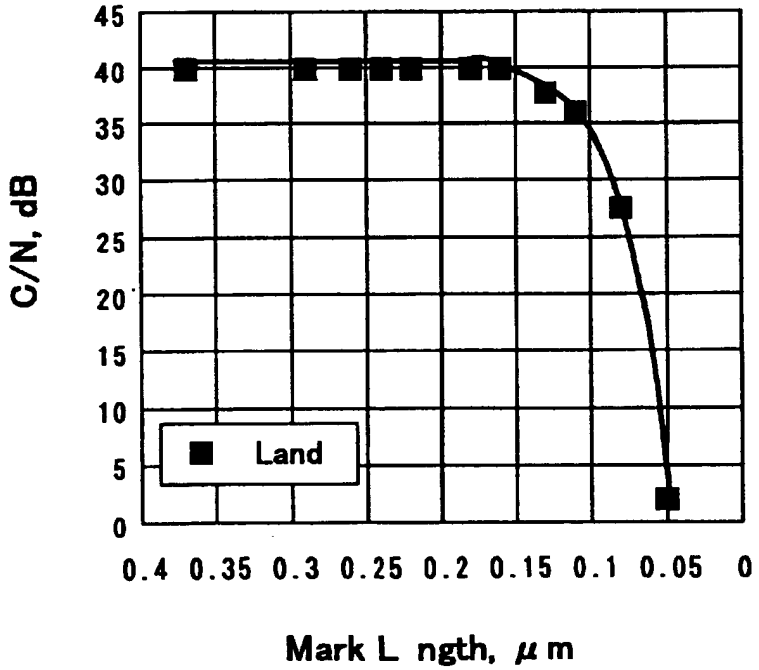
45
40
35
30
25
20
15
10
5
0
C/N, dB
Land
0.4 0.35 0.3 0.25 0.2 0.15 0.1 0.05 0
Mark L ngth, μm

Fig. 22

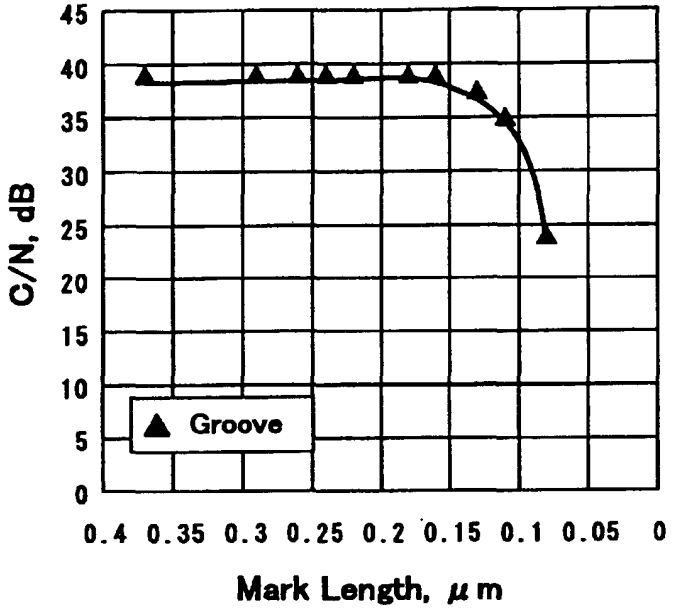

Fig. 23

W1	Wg	Dg	Wc	Dc
0.51 μm	0.51 μm	0.06 μm	0.04 μm	0.10 μm

Fig. 24

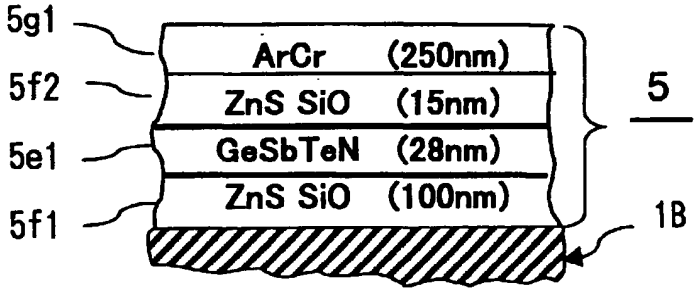

Fig. 25

	J1	J2	J3
Groove	6.9%	7.2%	7.5%
Land	7.4%	7.6%	8.0%

Fig. 26

	J1	J2	J3
Groove	6.7%	13.4%	24.0%
Land	7.5%	11.5%	16.5%

INFORMATION RECORDING MEDIUMS, SUPPORTER USED IN THE MEDIUMS, MANUFACTURE METHODS OF THE SUPPORTER, MANUFACTURING APPARATUS OF THE SUPPORTER AND STAMPERS FOR PRODUCING THE MEDIUMS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to information recording mediums such as discs, cards and tapes utilizing light or magnetization for recording/reproducing an information recording signal on/from the mediums, particularly, related to information recording mediums suitable for recording/reproducing type recording mediums utilizing magneto-optical or phase change phenomenon, support members (supporters) used for forming a recording layer of the medium thereon, manufacturing methods and apparatuses for manufacturing the supporters, and stampers for producing the mediums.

2. Description of the Related Arts

In the field of optical discs in the prior arts, there are recording/reproducing type discs such as a MD (mini disc) capable of recording music information and a DVD (digital versatile disc)-RAM capable of recording data. Further, recently, in even the field of floppy discs, which were only utilized in magnetic recording in the prior art, there has been developed an optical floppy disc. As a typical example, there has been developed an optical floppy referred to as a supper-disc employing an optical tracking. Furthermore, in the field of the cards in the prior art, the magnetic card was a main stream of the cards. Recently, however, an optical card is beginning to be seen in the market. Further, in even the field of the magnetic tapes there have been developed not only magnetic tapes but also optical tapes.

As mentioned above, the optical techniques are not a monopoly on the disc type information recording mediums but are applied to all kinds of recording mediums having various shapes. In any cases, the developments of the recording mediums are forwarded to realize a high recording density and large capacity recording.

In order to realize a high density recording of the optical disc, there are utilized optical techniques such as a super-resolution reproducing techniques and a land/groove recording technique. However, many problems are pointed out in these techniques, resulting in constraints on realizing a further high recording density.

Next, a description is given of an example of the super-resolution reproducing, i.e., a DWDD (Domain Wall Displacement Detection) type information recording medium and its problems.

Specifically, the DWDD type information recording medium refers to magneto-optical information recording medium such as a magneto-optical disc and a magneto-optical cards, wherein on a supporter member (referred to as a supporter hereinafter) a recording layer and a protection layer are laminated in this order. The recording layer comprises a displacement layer having a small wall coercivity, a switching layer having a relatively lower Curie temperature Ts and a memory layer having a relatively large wall coercivity, resulting an exchange-coupling triple-layered magnetic film known as a super-resolution layer.

Upon reproducing, when the recording layer is heated by being locally irradiated with a laser beam thereon, a temperature gradient is developed in the recording layer. This temperature gradient causes force to drive the domain wall of the displacement layer against the wall coercivity thereof in the higher temperature direction because the wall energy decreases as the temperature increases. When the domain wall of the displacement layer is located in a region where the temperature is lower than the temperature Ts, the domain wall can not be displaced due to the large frictional force from the memory layer through the exchange coupling acting between the displacement layer and the memory layer through the switching layer. However, along with the laser beam movement, when the domain wall is transferred into a region where the temperature is higher than the temperature Ts, the exchange coupling between the displacement layer and the memory layer through the switching layer is disappeared because the magnetization of the switching layer is vanished, and as a result, the domain wall in the displacement layer is solely displaced in the higher temperature direction. The domain wall displacement in the displacement layer is developed each time when a domain wall which is formed at an interval corresponding to an information signal, reaches the isothermal line of the Ts.

In other words, as the recording medium is scanned at a constant speed by using the laser beam, this domain wall displacement mentioned above occurs at a time interval corresponding to a spatial interval of the recorded domain wall. Thus, the information recording signal is reproduced by detecting magnetic reversals associated with the domain wall displacement by using a conventional magneto-optical system irrespective of the resolution of an optical readout system used in the apparatus.

FIG. **5** is a schematic sectional view of a supporter used in an information recording medium in the prior art, and FIG. **6** is a schematic sectional view of an information recording medium employing the supporter shown in FIG. **5** in the prior art.

FIG. **5** shows a supporter **7** used for a DWDD type information recording medium, and FIG. **6** shows the DWDD type information recording medium employing the DWDD type supporter **7** shown in FIG. **5** on which a recording layer **5** and a protection layer **6** are laminated in this order.

Referring to FIG. **5**, on the supporter **7** there are formed optical tracking grooves (referred to as grooves hereinafter) **3** having a flat bottom, as a minute track pattern. For example, in a case where the supporter **7** is used for a disc-type information recording medium such as an optical disc, the grooves **3** are formed circularly or spirally. And, between adjacent grooves **3**, there is formed a flat hill referred to as a land **2**. As shown in FIG. **6**, on a plane of the supporter **7** formed with the land **2** and the grooves **3**, there are formed a recording layer **5** and a protection layer **6**, resulting in an information recording medium A. The recording layer **5** is made of a super-resolution magneto-optical layer, for instance, a triple-layered film composed of a displacement layer made of GdFeCr, a switching layer of TbFeCr and a memory layer of TbFeCoCr.

In order to derive the excellent characteristics from this recording layer to a maximum, the recording layer **5** may be interposed between subsidiary dielectric layers. Here, the recording layer including the subsidiary layers is designated as the recording layer **5**. The protection layer **6** is provided for protecting the recording layer **5**, and is made of a thick resin layer made of an ultraviolet curing resin or a heat curing resin.

As to a principle of the DWDD, it is explained in detail in 1998 National Convention Record, the Institute of Elec-

trical Engineers of Japan, S. 10-7 (page, S. 10–25 to 28). Thus, a detailed explanation thereof is omitted here for simplicity. However, it should be noted that an information signal is recorded on either a group of the lands **2** or a group of the grooves **3**. At that time, either the group of the lands **2** or the group of the grooves **3** is made to be a non-magnetic area and the other is made to be a magnetic area. One of the most significant points to realize the DWDD reproducing is that a designed super-resolution phenomenon is never developed as far as both the group of the lands **2** and the group of the grooves **3** are made to be the magnetic area. In other words, the DWDD is not developed in the information recording medium A shown in FIG. **6** as it is. Thus, it is necessary to convert a part of the magnetic area into a non-magnetic area corresponding to non-recording tracks by continuously heating the part of the magnetic area with a laser beam from a recording/reproducing pickup at a higher power than that used in the recording.

FIG. **7** is a schematic sectional view showing a state where the lands of the DWDD type information recording medium shown in FIG. **6** are annealed, wherein the grooves **3** are made to be recorded tracks and the lands **2** are made to be non-magnetic tracks.

Specifically, before recording an information signal on the grooves **3**, the magnetic area of the lands **2** is converted into a non-magnetic area by continuously scanning the lands **2** with the laser beam at a higher power L than that used in the recording. This process is referred to as a laser annealing process hereinafter. In FIG. **7**, a hatched portion represents an annealed portion. Thus, the magnetic coupling between the lands **2** and the grooves **3** are disconnected, resulting in a DWDD type information recording medium **40**. After the laser annealing process, it is possible to record/reproduce an information signal on/from the grooves **3**, resulting in a development of the super-resolution phenomenon in the reproducing. This means that it is possible to read out a recorded information signal having a signal length smaller than that of the optically readable minimum signal length which is calculated by using both a wavelength of a laser beam and a numerical aperture of an objective lens used in the reproducing process.

The DWDD technique mentioned above is an excellent super-resolution recording/reproducing technique in principle, however, there is no alternative but the laser annealing to disconnect the magnetic coupling between the lands **2** and the grooves **3**. This fact causes a problem of poor mass-productivity of the information recording medium. For instance, it takes a long time of 30 to 90 minutes for the laser annealing process because every track has to be scanned with the laser beam. Further, there is a theoretical problem that it is impossible to record an information signal on both the lands **2** and the grooves **3** because it requires an alternate construction of the magnetic area and the non-magnetic area. Thus, such a land/groove recording as utilized in a DVD-RAM can not be realized, resulting in a limitation to realize a large capacity recording.

SUMMARY OF THE INVENTION

Accordingly, it is a general object of the present invention to provide an information recording medium in which the above disadvantages have been eliminated.

It is a more specific object of the present invention to provide information recording mediums capable of recording information signals on both lands and grooves and having a large recording capacity and a high mass-productivity without the laser annealing process, supporters used for the information recording mediums, manufacturing methods for the supporters, manufacturing apparatus for the supporters and stampers for producing the information recording mediums.

It is another object of the present invention to provide an information recording medium for recording an information signal thereon comprising: a supporter on which lands and grooves are alternately formed as a minute track pattern, a crevice, at least, formed in the respective grooves, the crevice having a depth larger than that of the respective grooves, and a recording layer formed on the supporter.

It is still another object of the present invention to provide an information recording medium for recording an information signal thereon comprising: a supporter on which lands and grooves are alternately formed as a minute track pattern; two crevices formed in the respective grooves nearby both ends of the respective grooves in a width direction of the respective grooves, the two crevices having a depth larger than that of the respective grooves, and a recording layer formed on the supporter.

It is a further object of the present invention to provide an supporter used for forming a recording layer of an information recording medium thereon, wherein lands and grooves are alternately formed in the supporter as a minute track pattern, and, at least, one crevice having a depth larger than that of the respective grooves is formed in the respective grooves.

It is a still further object of the present invention to provide an supporter used for forming a recording layer of an information recording medium thereon, wherein lands and grooves are alternately formed in the supporter as a minute track pattern, and two crevice having a depth larger than that of the respective grooves, are formed in the respective grooves nearby both ends thereof in a width direction of the respective grooves.

It is another object of the present invention to provide a manufacture method of an supporter used for forming a recording layer of an information recording medium thereon comprising the steps of: forming a patterning mask having an dry-etching proof on a support member polished in high precision and cleaned; forming a pattern corresponding to the minute track pattern on the patterning mask on the support member; forming the grooves and the crevice at the same time by a dry-etching method under a gas pressure of 35 to 500 mtorr; and, removing the patterning mask remained.

A further object of the present invention is to provide a manufacture apparatus for manufacturing a supporter used for forming a recording layer of an information medium thereon, wherein the manufacture apparatus has means for simultaneously forming grooves and crevices in the supporter according to a minute track pattern formed thereon by dry-etching.

A still further object of the present invention is to provide a stamper used for producing a supporter for forming a recording layer of an information recording medium thereon, wherein lands and grooves are alternately formed on the stamper, and a crevice having a height larger than that of the respective grooves is, at least, formed in the respective grooves.

Another object of the present invention is to provide a manufacturing method of a supporter for forming a recording layer of an information recording medium thereon, comprising the steps of forming a glass master, producing a stamper from the glass master and forming the supporter with the stamper, wherein the glass master forming process

comprises the steps of: forming a patterning mask having a dry-etching proof on a support base polished in high precision and cleaned; forming a pattern corresponding to a minute track pattern on the patterning mask formed on the support base; forming grooves and crevices in the support base at the same time according the pattern by dry-etching under the gas pressure of 35 to 500 mtorr; and removing the patterning mask remained from the support base.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic sectional view of a supporter of a first embodiment used for an information recording medium in the present invention;

FIG. **2** is a schematic sectional view of an information recording medium of a first embodiment in the present invention;

FIG. **3** is a schematic sectional view of a supporter of a second embodiment used for an information recording medium in the present invention;

FIG. **4** is a schematic sectional view of an information recording medium of a second embodiment in the present invention;

FIG. **5** is a schematic sectional view of a supporter used in an information recording medium in the prior art;

FIG. **6** is a schematic sectional view of an information recording medium employing the supporter shown in FIG. **5** in the prior art;

FIG. **7** is a schematic sectional view showing a state where the lands of the DWDD type information recording medium shown in FIG. **6** are annealed;

FIG. **8** is a chart showing dimensions of constructive parts of the support shown in FIG. **1**;

FIG. **9** is a section of a recording layer for explaining a concrete lamination structure of the recording layer in the present invention;

FIG. **10** is a chart showing dimensions of constructive parts of the supporter of the second embodiment shown in FIG. **3**:

FIG. **11** is a section of another recording layer for explaining a concrete lamination structure of the recording layer in the present invention;

FIG. **12** is a graph showing a mark length vs C/N reproducing characteristic of the information recording medium of the first embodiment shown in FIG. **2**;

FIG. **13** is a graph showing a mark length vs C/N reproducing characteristics as the land recording of the information recording medium of the second embodiment;

FIG. **14** is a graph showing a mark length vs C/N reproducing characteristics as the groove recording of the information recording medium of the second embodiment;

FIGS. **15** (*a*) to **15** (*e*) are schematic sectional views for explaining a manufacturing process of the supporter of a first embodiment shown in FIG. **1** in the present invention;

FIGS. **16** (*a*) to **16** (*e*) are schematic sectional views for explaining a manufacturing process of the supporter of the second embodiment shown in FIG. **3** in the present invention;

FIG. **17** is a schematic view for explaining a structure of a dry etching apparatus used in the manufacturing process of the supporter;

FIG. **18** is a schematic view for explaining a structure of another dry etching apparatus used in the manufacturing process of the supporter;

FIGS. **19** (*a*) to **19** (*i*) are schematic sectional views for explaining a manufacturing process of the supporter of a third embodiment **3** in the present invention;

FIG. **20** is a section of other recording layer for explaining a concrete laminated structure of the recording layer in the present invention;

FIG. **21** is a graph showing a mark length vs C/N reproduction frequency characteristic on a land recording of an information recording disc in the present invention;

FIG. **22** is a graph showing a mark length vs C/N reproduction frequency characteristic on a groove recording of an information recording disc in the present invention;

FIG. **23** is a chart showing concrete dimensions of the surface shape of the supporter in the present invention;

FIG. **24** is a section showing a recording layer for explaining other concrete laminated structure of the recording layer in the present invention.

FIG. **25** is a chart showing measurement values of jitter on the land/groove recording in the present invention; and

FIG. **26** is a chart showing measurement values of jitter on the land/groove recording in the prior art.

Through the drawings, like parts are designated with like reference characters, and a detailed description thereof is omitted for simplicity.

DETAILED DESCRIPTION OF THE PREFEREED EMBODIMENTS

Description is given in detail of embodiments of information recording mediums of the present invention, supporters used for the information recording mediums, manufacturing methods for the supporters, manufacturing apparatuses for the supporters and stampers for producing the information recording mediums in the present invention.

FIG. **1** is a schematic sectional view of a supporter of a first embodiment used for an information recording medium in the present invention;

FIG. **2** is a schematic sectional view of an information recording medium of a first embodiment in the present invention;

FIG. **3** is a schematic sectional view of a supporter of a second embodiment used for an information recording medium in the present invention;

FIG. **4** is a schematic sectional view of an information recording medium of a second embodiment in the present invention;

FIGS. **15** (*a*) to **15** (*e*) are schematic sectional views for explaining a manufacturing process of the supporter of the first embodiment shown in FIG. **1** in the present invention;

FIGS. **16** (*a*) to **16** (*e*) are schematic sectional views for explaining a manufacturing process of the supporter of the second embodiment shown in FIG. **3** in the present invention;

FIGS. **19** (*a*) to **19** (*i*) are schematic sectional views for explaining a manufacturing process of the supporter of a third embodiment in the present invention;

FIG. **17** is a schematic view for explaining a structure of a dry etching apparatus used in the manufacturing process of the supporter;

FIG. **18** is a schematic view for explaining a structure of another dry etching apparatus used in the manufacturing process of the supporter;

Through the drawings, like parts are designated with like reference characters, and a detailed description thereof is omitted for simplicity.

The present inventions have been obtained by studying the problems mentioned in the foregoing.

Specifically, in the DWDD type information recording medium **40** in the prior art shown in FIG. **7**, the reason why the lands **2** have to be non-magnetized depends on a fact that the recording layer **5** is faithfully formed as one layer on the supporter **7** in accordance with a surface shape of the supporter by continuously forming the lands **2** and the grooves **3** without a gap, otherwise, in order to save the laser annealing process, the recording layer needs to be cut at every recording track. However, it is impossible to form designed discrete tracks by using a sputtering method utilized in forming the magneto-optical layer such as the recording layer **5** because of its good diffusion or invading characteristic of sputtered materials.

According to the present invention, it is possible to provide a supporter capable of forming a recording layer **5** having discrete tracks (capable of forming a gap between a groove **3** and a land **2** adjacent to each other) by employing a conventional thin-layer forming apparatus. Further, it is possible to provide an information recording medium having the discrete tracks by utilizing the support mentioned above.

A supporter **1A** of a first embodiment in the present invention is shown in FIG. **1**. As seen from FIG. **1**, on a surface of the supporter **1A**, grooves **3** and lands **2** are alternately formed in the same manner as those of the supporter **40** in the prior art shown in FIG. **5**.

However, it should be noted that in the supporter **1A** of the first embodiment, there is provided one crevice **4** between a groove **3** and a land **2** adjacent to each other. A bottom surface of the groove **3** and a top surface of the land **2** are disposed to be parallel to each other, and there is provided one crevice **4** in each groove **3** disposed between the adjacent lands **2**.

Here, the crevice **4** refers to a concave shape formed or bored in the groove **3** of the supporter **1A** at a position lower than that of the bottom surface of the groove **3**. A depth Dc of the crevice **4** is larger than a depth Dg of the groove **3** (Dc>Dg). The crevice **4** has a section of an inverse rectangular, i.e., a sharp V-letter ditch. When the sharp V-letter ditch is observed from an outside thereof, it seems to be a crevice Thus, it is named a crevice after its shape by the present inventor. In FIG. **1**, a reference character W1 designates a width of the land **2**, Wc a width of the crevice **4** and Wg+Wc a width of the groove **3**.

In this embodiment, the crevice **4** is formed nearby one end **3***a* of the groove **3** in a width direction of the groove **3**. However, the crevice **4** may be formed nearby the other end **3***b* though it not depicted. Further, the crevice **4** may be formed nearby a center portion in the groove **3** as a single one or plural ones, each having a sharp V-letter ditch, if necessary.

In other words, the supporter **1A** of the present invention used for an information recording medium is applied to an information recording medium B (shown in FIG. **2**) of the present invention, and has constructive features that it is formed with the lands **2** and grooves **3** alternately formed on the surface thereof as a minute track pattern. In addition, the respective grooves are formed with a crevice **4** having a depth Dc larger than that of the groove **3** nearby one end **3***a* or the other end **3***b* of the respective grooves **3** in the width direction of the groove **3**.

In summary, a supporter for an information recording medium according to the present invention is used for an information recording medium according to the present invention, and has constructive features that it has the lands **2** and the grooves **3** alternately formed thereon as a minute track pattern, and, at least, one crevice **4** having a depth Dc larger than a depth Dg of the respective grooves **3** is formed in the respective grooves **3**.

As shown in FIG. **2**, the information recording medium B of the present invention comprises the supporter **1A** shown in FIG. **1**, a recording layer **5** formed on the supporter **1A** and a protection layer **6** on the recording layer **5**, which are laminated in this order.

Here, the recording layer **5** is formed on a surface of the supporter **1A** by a sputtering method, however, sputtered materials from a sputtering apparatus are not attached in the crevice **4** because the crevice **4** itself becomes a shadow for the sputtering, resulting in that the recording layer **5** is scarcely formed in the crevice **4**, even when the sputtering apparatus has a good diffusion or invading characteristic of the sputtered materials.

Accordingly, the recording layer **5** has such a shape as being cut nearby the respective crevices **4**. Only one crevice **4** is formed in the respective grooves **3**. Thus, a number of effective recording tracks coincides with the number of the lands **2** (referred to as a land recording).

On the other hand, the protection layer **6** is formed as a thick layer on the recording layer **5** by a spin coating method, resulting in a continuous flat layer thereon. However, it should be noted that an important thing is that the recording layer **5** is discontinuously formed. The continuous construction of the protection layer **6** does not interfere with the recording layer **5**.

In other words, the information recording medium B of the present invention has constructive features as follows.

On the supporter **1A** of the present invention, at least, a recording layer **5** is formed. In addition, the lands **2** and grooves **3** are alternately formed on the supporter **1A** as a minute recording track pattern. Further, at least, one crevice **4** having a depth Dc larger than a depth Dg of the respective grooves **3** is formed within the respective grooves **3** nearby one end **3***a* (or **3***b*) of the respective grooves **3** in the width direction thereof.

In summary, the information recording medium of the present invention has constructive features that on the supporter of the present invention, at least, a recording layer **5** is formed, and the lands **2** and grooves **3** are alternately formed on the supporter as a minute recording track pattern, and, at least, one crevice **4** having a depth Dc larger than a depth Dg of the respective grooves **3** is formed within the respective grooves **3**.

As shown in FIG. **3**, a supporter **1B** of a second embodiment in the present invention has a alternately repeated construction of a land **2** and a groove **3** adjacent to the land **2** in the same manner as mentioned in the prior art, and is formed with a pair of crevices **4**, **4** in the respective grooves **3** nearby both ends of the respective grooves **3** in a width direction thereof. Each of the pair of crevices **4**, **4** is formed in the groove **3** at a position lower than that of a bottom surface of the groove **3** so that a depth Dc of the crevice **4** is larger than a depth Dg of the groove **3**, and is formed to have an inverse rectangular in section, i.e., a sharp V-letter shape in section as mentioned in the foregoing.

In FIG. **3**, a reference character Wl represents a width of the land **2**, Wc a width of the crevice **4** and Wg+2Wc a width of the groove **3**.

In other words, the supporter **1B** of the second embodiment in the present invention used for an information recording medium is applied to an information recording medium C (shown in FIG. **4**) of a second embodiment in the present invention, and has constructive features that it is

alternately formed with the lands **2** and grooves **3** thereon as a minute track pattern. Further, in the respective grooves **3** there are formed a pair of crevices **4**, **4** each having a depth Dc larger than a depth Dg of the groove **3** nearby both ends **3***a*, **3***b* of the respective grooves **3** in the width direction of the groove **3**.

As shown in FIG. **4**, the information recording medium C of the second embodiment in the present invention has the supporter **1**B shown in FIG. **3**, a recording layer **5** formed on the supporter **1**B and a protection layer **6** on the recording layer **5**, which are laminated in this order. Here, the recording layer **5** is formed by a sputtering method, however, sputtered materials from a sputtering apparatus are not attached in the crevice **4** because the crevice **4** itself becomes a shadow for the sputtering, resulting in that recording layer **5** is scarcely formed in the crevice **4** even when the sputtering apparatus has a good diffusion or invading characteristic of the sputtered materials. Accordingly, the recording layer **5** has such a shape as being cut nearby the respective crevices **4**. Two crevices **4** are formed in the respective grooves **3**. Thus, a number of effective recording tracks coincides with a sum of a number of the lands **2** and a number of the grooves **3** (referred to as a land/groove recording).

On the other hand, the protection layer **6** is formed as a thick layer on the recording layer **5** by a spin coating method, resulting in a continuous flat layer thereon. However, it should be noted that an important thing is that the recording layer **5** is discontinuously formed. The continuous construction of the protection layer **6** does not interfere with the recording layer **5**.

As mentioned above, according to the information recording medium C of the second embodiment in the present invention it is possible to realize a land/groove recording which was impossible in the prior art, resulting in a double recording capacity compared to that of the recording medium B of the first embodiment shown in FIG. **2**.

In other words, the information recording medium C of the present invention has constructive features as follows.

On the supporter **1**B mentioned in the foregoing there is formed, at least, a recording layer **5**. In addition, the lands **2** and grooves **3** are alternately formed on a surface of the supporter as a minute recording track pattern. Further, a pair of crevices **4** each having a depth Dc larger than a depth Dg of the respective grooves **3** is formed within the respective grooves **3** nearby both ends **3***a*, **3***b* of the respective grooves **3** in the width direction thereof.

Further, as mentioned in the foregoing, in the information recording medium B of the first embodiment shown in FIG. **2**, the recording layer **5** formed on the supporter **1**A was cut into a plurality of recording areas **5***c* every minute recording track.

On the other hand, in the information recording medium C of the second embodiment shown in FIG. **4**, the recording layer **5** formed on the supporter **1**B is cut into a plurality of recording areas **5***d* every minute recording track.

Furthermore, the recording layer **5**, as a constructive member of the recording medium A or B, has, at least, a super-resolution recording layer, and this super-resolution recording layer is made of the DWDD type super-resolution magneto-optical recording layer of a triple-layered film composed of the displacement layer, the switching layer and the memory layer as mentioned in the foregoing.

Next, the description is given of the recording mediums of concert embodiments 1 to 4 in the present invention.

[Embodiment 1]

An example of a card type information recording medium formed with the lands and the grooves in parallel.

A supporter **1**A made of a quartz glass plate of 85 mm ×54 mm×0.7 mm was prepared. The schematic sectional view of the supporter **1**A is shown in FIG. **1**, wherein the lands **2**, the grooves **3** and the crevices **4** are formed as mentioned in the foregoing.

FIG. **8** is a chart showing dimensions of constructive parts of the support shown in FIG. **1**.

The dimensions of constructive parts of the supporter **1**A are shown in FIG. **8** in accordance with the reference characters shown in FIG. **1**.

Specifically, a width W1 of the land **2** is 0.55 μm, a width (Wg +Wc) of the groove is 0.55 μm, wherein the width Wg is 0.51 μm and the width Wc of the crevice **4** is 0.04 μm, a depth Dg of the groove **3** is 0.2 μm and a depth Dc of the crevice **4** is 0.35 μm.

Next, on the supporter **1**A, a recording layer **5** and a protection layer **6** were formed. The recording layer **5** was formed by a well known sputtering method.

FIG. **9** is a section of a recording layer for explaining a concrete lamination structure of the recording layer in the present invention.

Materials used for the recording layer **5** are shown in FIG. **9**. Specifically, the recording layer **5** was formed by sandwiching a magneto-optical layer of the triple-layered film (a displacement layer **5***a***1** of GdCo having a thickness of 30 nm, a switching layer **5***a***2** of DyFe having a thickness of 10 nm and a memory layer **5***a***3** of TbFeCo having a thickness of 40 nm) known as the DWDD. (Domain Wall Displacement Detection) type super-resolution layer between a first dielectric layer **5***a***4** of SiO having thickness of 100 nm and a second dielectric layer **5***a***5** of TaO having a thickness of 60 nm. Next, the protection layer **6** was formed on the recording layer **5** by coating a thermosetting resin at a thickness of 15 μm by a well known screen printing method. The protection layer was cured at a temperature of 80° C. by baking. This card was cut in a perpendicular direction to recording tracks. The section of the card was observed with a scanning electron microscope. As a result, it was confirmed that the section had the sectional shape as shown as shown in FIG. **2**.

FIG. **12** is a graph showing a mark length vs C/N reproducing characteristic of the information recording medium of the first embodiment shown in FIG. **2**.

Next, an information signal was recorded/reproduced on/from this card by irradiating and focusing a laser beam on the lands **2** thereof, resulting in that a reproducing characteristic of a mark length vs C/N was obtained as shown in FIG. **12**. In a recording apparatus used here, there were employed a laser beam having a wavelength of 780 nm and an objective lens having a numerical aperture of 0.55. In this case, a single frequency recording/reproducing was performed, however, it should be noted that no laser annealing was carried out. The recording power was 3.5 mW and the reproducing power was 1.9 mW. Upon reproducing it was confirmed that a super-resolution phenomenon was developed because a recording/reproducing of the shortest mark length of 0.08 μm was attained. Further, the C/N at a mark length of 0.1 μm was 34 dB which is a reproducing level enough for a practical use. In this connection, a reproducing limitation obtained from a theoretical calculation by using the wavelength and the numerical aperture is a mark length of 0.3 5 μm.

[Embodiment 2]

An example of an information recording disc, wherein a land and a groove are coaxially and spirally formed in parallel to each other.

A supporter 1B made of a soda lime glass plate having a diameter of 120 mm and a thickness of 0.6 mm was prepared. The schematic sectional view of the supporter 1B is shown in FIG. 3, wherein the land 2, the groove 3 having the crevices 4 are coaxially and spirally formed in parallel to each other.

FIG. 10 is a chart showing dimensions of constructive parts of the supporter of the second embodiment shown in FIG. 3.

The dimensional construction of the supporter 1B is shown in FIG. 10 in accordance with the reference characters shown in FIG. 3.

Specifically, a width W1 of the land 2 is 0.51 μm, a width (Wg+2Wc) of the groove 3 is 0.59 μm, wherein the width Wg is 0.51 μm and the width Wc of the crevice 4 is 0.04 μm, the depth Dg of the groove 3 is 0.2 μm and the depth Dc of the crevice 4 is 0.35 μm.

Next, on this supporter 1B, the recording layer 5 and the protection layer 6 were formed.

FIG. 11 is a section of another recording layer for explaining a concrete laminated structure of the recording layer in the present invention.

The recording layer 5 was made of recording materials shown in FIG. 11 by using a known sputtering method.

Specifically, the recording layer 5 was formed by sandwiching the DWDD type super-resolution layer such as the triple-layered magneto-optical film composed of the displacement layer 5b1 of GdFeCr (thickness of 30 nm), the switching layer 5b2 of TbFeCr (thickness of 10 nm) and the memory layer 5b3 of TbFeCoCr (thickness of 80 nm) between a first dielectric layer 5b4 of SiN (thickness of 90 nm) and a second dielectric layer 5b5 of SiN (thickness of 50 nm).

Next, the protection layer 6 was formed on the second dielectric layer 5b5 in such a manner that an ultraviolet curing resin was coated to be 6 μm by the well known thin film rotating forming method and was cured by irradiating ultraviolet rays thereon.

This information recording disc was cut in a perpendicular direction to the recording tracks, and the section of the disc was observed with a scanning electron microscope. Thus, it was confirmed that the section of the disc had a sectional shape as shown in FIG. 4.

FIG. 13 is a graph showing a mark length vs C/N reproducing characteristics as the land recording of the information recording medium of the second embodiment.

Next, an information signal was recorded/reproduced on/from this information recording disc by irradiating and focusing a laser beam on the lands 2 thereof, resulting in a reproducing characteristic of a mark length vs C/N as shown in FIG. 13. In the recording apparatus used here, there were employed a laser beam having a wavelength of 690 nm and an objective lens having a numerical aperture of 0.6, and a single frequency recording/reproducing was carried out. The recording power was 3.7 mW and the reproducing power was 2.2 mW. Upon reproducing it was confirmed that a recording of a mark length of 0.06 μm had been attained, resulting in a generation of a super-resolution phenomenon. Further, the C/N at a mark length of 0.1 μm was 36 dB which is a reproducing level enough for a practical use. In this connection, a reproducing limitation obtained from a theoretical calculation by using the wavelength and the numerical aperture is a mark length of 0.26 μm.

FIG. 14 is a graph showing a mark length vs C/N reproducing characteristics as the groove recording of the information recording medium of the second embodiment

Next, an information recording signal was recorded/reproduced on/from the grooves 3 by irradiating and focusing the laser beam on the grooves 3, resulting in a reproducing characteristic of a mark vs C/N as shown in FIG. 14. As seen from FIG. 14, it was confirmed that the shortest mark of 0.08 μm had been attained, resulting in a generation of the super-resolution phenomenon. Further, the C/N at a mark length of 0.1 μm is 35 dB which is a reproducing level enough for a practical use.

Thus, it should be noted that the land/groove recording has been realized in the information recording medium 1B of the second embodiment as mentioned referring to FIGS. 13 and 14.

As seen from the embodiments in the foregoing, the recording layer 5 can be automatically cut into every track by employing the supporter 1A or 1B having crevices 4 even when the conventional sputtering apparatus is utilized. Here, an important thing is that it is possible to separate the recording layer 5 into every track at a time when the sputtering thin layer forming process has been completed without an etching process. In other words, a self-cutting of the recording layer 5 is realized at every track. Thereby, it is possible to realize a high density recording/reproducing. Especially, it is possible to save the laser annealing for the super-resolution recording layer represented by the DWDD, resulting in a realization of the land/groove recording.

The above description has been given of the supporters used for the information recording mediums and the information recording mediums having the above supporters, however, the present invention is not limited to these embodiments. The materials and dimensions of the constructive members may be optionally changed if necessary.

In the present invention, the supporter to be used needs to be formed or bored with a minute track pattern having crevices 4, and can be made from various kinds of synthetic resins such as polycarbonate, poly (methyl methacrylate), polystyren, polycarbonate-polystyren copolymer, poly (vinyl chloride), alicylic polyolefin and poly (methyl pentene), and glasses such as a soda aluminosilicate glass and a borosilicate glass. Further, on the supporter 1A or 1B, pits, holograms or certified marks may be formed other than the lands 2 grooves 3 and crevices 4, if necessary.

As the materials of the recording layer 5, there may be used inorganic materials such as neodymium, dysprosium, bismuth, palladium, samarium, holmium, erbium, ytterbium, ruthenium, praseodymium manganese, titanium, aluminum, silicon, indium, antimony, tellurium, selenium, arsenic, platinum, gold, silver, copper, tin, sulfur, and its alloys (including oxide, nitride and carbide) other than terbium, cobalt, iron, gadolinium and chromium.

Further, as the materials of the dielectric layers subsidiarily used, zinc, magnesium, calcium, aluminum, chromium, zirconium, fluorine, sulfur, and its alloys may be used other than silicon and tantalum.

Furthermore, as the materials of the reflective layer subsidiarily used, aluminum, gold, silver, copper, iron, zinc, chromium, tantalum, titanium, molybdenum, silicon and nickel, and its alloys may be laminated.

Further, as the materials of the protection layer 6, there may be employed various kinds of radiation (including

visible lights) curing resins, an electron beam curing resin, a moist curing resin and a mixing type curing resin other than the thermosetting resin or the ultraviolet ray curing resin. On the protection layer **6**, characters or the like may be printed, if necessary.

The wavelength of the laser beam used for recording or reproducing is not limited to 780 nm or 690 nm. It is possible to employ a wave length of 830, 650, 635, 532, 430, 410 or 370 nm. Further, as to the numerical aperture of the objective lens used for the apparatus, it is possible to employ 0.4, 0.45, 0.65, 0.7, 0.75, 0.8, 0.85, or 0.9.other than 0.55 and 0.6. Further, it is possible to employ a numerical aperture larger than 1 as typically seen in a solid immersion lens. Needless to say, it is possible to change the thickness and the structure of the respective layers **5**, **6** and the external dimensions of the supporter **1A** or **1B**, and its minute dimensions

The description has been given of the examples of the card and the disc as the information recording medium and the supporters for the mediums in the present invention. However, the present invention is not limited to these embodiments but applicable to others, for instance, to an optical floppy disc and an optical tape other than the card and the disc.

As the recording layer **5** used in the Embodiments 1 and 2, the DWDD type super-resolution layer is employed, however, the recording layer of the present invention is not limited to it. Other super-resolution layers based on other reproducing principles may be employed for it.

Next, a description is given of manufacturing methods of the supporters **1A** and **1B** of a first and second embodiment in the present invention.

The dimensions of the respective crevices **4** formed on the supporter are smaller than those of the lands **2** and grooves **3** formed as a minute track pattern. Further, the respective crevices **4** need to be formed at a precise position in the respective grooves **4**. If a conventional photo-etching method is employed to form the minute track pattern and the crevices **4**, there are needed two processes, a groove forming process and a crevice forming process, resulting in a problem of a difficulty of the positional adjustment.

In the manufacture method of the supporter in the present invention, the above problem has been eliminated by forming the crevices **4** and the grooves **3** at the same time on the supporter by a dry etching method.

The manufacture method of the supporters **1A** and **1B** of the first and second embodiments in the present invention generally has a series of processes (a) to (e) as follows:

(a) preparing a supporter **1** polished in high precision and cleaned;

(b) forming a patterning mask **8** on the supporter **1** by coating a mask material having a dry etching proof;

(c) forming a pattern approximately corresponding to a necessary minute track pattern by a conventional photolithography method, wherein a flat portion **9** approximately corresponds to a position of a land **2**, and an opening portion **10** approximately corresponds to a position of both a groove **3** and a crevice **4** after all the processes are completed;

(d) forming the groove **3** and crevice **4** at the same time in the opening portion **10** of the pattern formed on the supporter **1** by a dry etching method with a special dry etching apparatus AA or BB according to the present invention, and

(e) removing the patterning mask **8** remaining on the supporter **1**, resulting in the supporter **1A** or **1B** shown in FIG. **1** or **3**.

In the above processes, the important things reside in special etching methods or apparatuses for simultaneously forming the groove **3** and crevice **4**.

These methods and apparatuses are explained in detail through an example of the supporter **1A** explained in the Embodiment 1 and the supporter **1B** explained in the Embodiment 2 mentioned in the foregoing.

FIGS. **15** (*a*) to **15** (*e*) are schematic views for explaining a manufacturing method of the supporter of the first embodiment shown in FIG. **1** in the present invention,

FIG. **17** is a schematic view for explaining a dry etching apparatus of the present invention.

First, a description is given of a manufacturing method of a first embodiment through an example of the supporter **1A** (FIGS. **1** and **8**) on processes (1) to (5) mentioned below, referring to FIGS. **15** (*a*) to **15** (*e*).

(1) preparing a supporter **1** having a mirror surface made of a quartz glass plate (85 mm×54 mm×0.7 mm) of which surface is polished in high precision and cleaned (FIG. **15** (*a*));

(2) forming a patterning mask **8** on the supporter **1** by uniformly coating chromium as the patterning mask **8** (FIG. **15**(*b*));

(3) forming a pattern on the patterning mask **8** corresponding to a necessary minute track pattern by the conventional photolithography (FIG. **15** (*c*)). Specifically, a photo-resist was coated as a thin layer on the patterning mask **8**. After a negative-film having a parallel pattern of line and space was superimposed on the thin layer of the photo-resist, an exposure and development were performed (not shown). Successively, the patterning mask **8** on the supporter was selectively removed by a wet etching method i.e., by dipping the supporter **1** into a mixed solution of 2-cerium ammon and glacial acetic acid, resulting in a pattern of the patterning mask **8** having flat portions **9** having a width of 0.55 μm and opening portions **10** having a width of 0.55 μm after the photo-resist remained was removed.

(4) The supporter **1** was placed on a substrate electrode **22** of a parallel plate type dry etching apparatus AA shown in FIG. **17** of the present invention. Then, the opening portions **10** of the patterning mask **8** were dry-etched by using CF4 gas (FIG. **15** (*d*)).

(5) After etched, the patterning mask **8** was removed by dipping the supporter **1** into a mixed solution of 2-cerium ammon and glacial acetic acid, resulting in the supporter **1A** (FIG. **15** (*e*)).

In the above process (4), the dry etching process was performed by using a dry etching apparatus AA shown in FIG. **17**. The dry etching apparatus AA is provided with means for simultaneously forming or boring the grooves **3** and the crevices **4** in the supporter **1** at positions corresponding to the opening portions **10** of the patterning mask **8** by dry-etching, as mentioned hereinafter.

The dry etching apparatus AA has a construction of a parallel plate type etching apparatus. Specifically, referring to FIG. **17**, a reference character **1** represents the supporter having a mirror surface to be dry-etched as a sample, and the supporter **1** to be dry-etched is placed on a substrate electrode **22**. A reference character **23** represents a first valve installed in a vacuum exhaust system channel **23***a*, **24** a second valve installed in an etching gas exhaust system channel **24***a*, **25** a conductance valve installed in a channel formed between a chamber **26** and the first and second valves **23**, **24**.

A reference character **27** represents a flowmeter, and **28** a high frequency power source. A reference character **29** represents an etching gas inlet of which one end is connected to the flowmeter **27** and of which another other end is protruding into the chamber **26, 20** an opposed electrode as a grounded pole which is fixed in a position apart from the substrate electrode **22** at a predetermined distance, and **21** a gas bomb for dry-etching. Further, the etching gas inlet **29** is disposed approximately at an opposite side of the conductance valve **25**, resulting that the supporter **1** to be dry-etched stands between the etching gas inlet **29** and the conductance valve **25**. Thus, the etching gas flows over the support **1** from the gas inlet **29** to the etching gas exhaust system **24***a* through the conductance valve **25**. Incidentally, the substrate electrode **22** is cooled down at temperature of 22°**0** C.

A dry-etching process of the supporter **1** to be try-etched is successively performed with the dry etching apparatus AA according to the following processes (1) to (3). After the supporter **1** as a sample is placed on the substrate electrode **22**, the chamber **26** is evacuated in a high vacuum level by opening the first valve **23** installed in the high vacuum exhaust system **23***a* and closing the second valve **24** installed in the etching gas exhaust system **24***a* and operating the conductance valve (CV) **25**. Next, the high vacuum exhaust system **23***a* is changed into the etching gas exhaust system **24***a* by a closing the first valve **23** and opening the second valve **24**. In this state, the etching gas is introduced into the chamber **26** from the gas bomb **21** through the flowmeter **27** and the etching gas inlet **29**. After the flowmeter **27** and the conductance valve **25** are adjusted so that the chamber **26** satisfies predetermined conditions, the supporter **1** as the sample is dry-etched with a plasma developed by applying a high frequency voltage from the high frequency power source **28** between the substrate electrode **22** and the opposed electrode **20**. Thus, it is possible to dry-etch the supporter **1** corresponding to the opening portions **10** of the patterning mask **8** by using the dry etching apparatus AA.

Here, a description is given of the reason why the groove **3** and the crevice **4** are formed at the same time by the dry etching method with the dry etching apparatus AA.

The crevice **4** shown in FIG. **1** is not formed at both sides of the groove **3** therein but only at one side thereof. This reason is not sufficiently made clear, however, it seems that the development of the crevice **4** is related to a flow of the etching gas.

Specifically, a boundary where the crevice **4** resides corresponds to an up-stream side of the etching gas (a side of the gas inlet **29**) and a boundary where the crevice **4** does not reside corresponds to a down-stream side of the etching gas (a side of the conductance valve **25**). The reason for the development of the crevice **4** is not definitely clear as mentioned above, however, when the etching gas is unequally provided in the chamber **26** like as this apparatus, the respective crevices **4** are unevenly distributed at only a predetermined one side of the respective grooves **3**. It is considered that in the plasma gas, both decomposition (etching) and accumulation (recombination of etched materials with the sample to be etched) are simultaneously developed, and its balance is broken when the etching gas is unevenly provided into the chamber **26**, resulting in the uneven distribution of the crevices **4**.

Under various kinds of etching conditions, the etching experiments were tried by the inventor, and a good experimental result was obtained of the supporter 1A shown in FIGS. **1, 8** under following dry-etching conditions.

etching gas: CHF3

gas pressure: 60 mtorr

gas flow rate: 57 sccm

etching time: 3 minutes 30 seconds

FIGS. **16** (*a*) to **16** (*e*) are schematic views for explaining a manufacturing method of the supporter of the second embodiment shown in FIGS. **3**; and

FIG. **18** is a schematic view for explaining another etching apparatus used in the manufacturing method shown in FIGS. **16** (*a*) to **16** (*e*) in the present invention.

Next, the description is given of a manufacture method of a second embodiment through an example of the supporter 1B shown in FIGS. **3, 10**, referring to FIGS. **16** (*a*) to **16** (*e*), wherein like components are shown with like reference characters and the detailed descriptions thereof are omitted for simplicity. Specifically,

(1) There was prepared a mirror supporter **1** made of a soda lime glass plate (a diameter of 120 mm and a thickness of 0.6 mm) of which surface is polished in high precision and cleaned (FIG. **16** (*a*)).

(2) A patterning mask **8** was formed on the mirror supporter **1** by uniformly coating photo-resist thereon (FIG. **16**(*b*)).

(3) A pattern corresponding to a necessary minute track pattern was formed by a conventional laser beam recording method (FIG. **16** (*c*)). Specifically, a spiral groove pattern was recorded on the photo-resist as the patterning mask **8** by irradiating and focusing a laser beam thereon with an objective lens, and the photo-resist was developed(not shown) Thereby, there was obtained a pattern having flat portions **9** having a width of 0.5 μm and opening portions **10** having a width of 0.6 μm.

(4) The supporter **1** mentioned above was set in the parallel plate type dry etching apparatus BB shown in FIG. **18**, and the dry etching was performed on the supporter **1** at positions corresponding to the opening portions **10** of the patterning mask (FIG. **16** (*d*)).

(5) After dry etching, the patterning mask **8** was removed by ashing with oxygen plasma, resulting in the supporter 1B (FIG. **16** (*e*)).

In the above manufacture processes of the supporter 1B, the dry etching process (5) is performed by using the dry etching apparatus BB shown in FIG. **18**. The dry etching apparatus BB has means for simultaneously forming or boring the grooves **3** and the crevices **4** in the surface of the supporter **1** at positions corresponding to the opening portions **10** of the patterning mask **8** by dry-etching.

The dry etching apparatus BB has a similar construction to the dry etching apparatus AA mentioned in the foregoing, however, an etching gas providing structure this apparatus BB is different from that of the dry etching apparatus AA. Specifically, in the dry etching apparatus BB, there are circularly disposed a plurality of etching gas inlets **29** around the mirror supporter **1** to be etched, so that the plurality of etching gas inlets **29** are allowed to provide the etching gas to the mirror supporter **1** from every direction. Other constructions of the apparatus BB are the same as those of the dry etching apparatus AA. The dry etching processes by using the dry etching apparatus BB are approximately the same as the processes (1) to (5) by using the dry etching apparatus AA, as mentioned in the foregoing, thus, the detailed explanation thereof is omitted here.

Next, the description is given of the reason why the grooves **3** and the crevices **4** are simultaneously formed by using the dry etching apparatus BB.

As mentioned in the foregoing, in the dry etching apparatus BB, the etching gas is provided to the supporter **1** from every direction. In this case, ions have an inclination to concentrate to a pointed portion, for instance, a boundary portion between the flat portion **9** and the opening portion **10**. This inclination is remarkably enhanced at a high etching gas pressure.

Accordingly, in the present invention, in order to form the crevice **4** at both sides of the opening portion **10**, a high etching gas pressure, which is not employed in a conventional dry etching method, is employed. The high etching gas pressure refers to a gas pressure of not lower than 35 mtorr. It has been confirmed by the present inventor through his experimental efforts that the dry etching was remarkably enhanced at the both side of the respective opening portions **10** because of the ion concentration thereto only when the etching gas pressure was made to be not lower than 35 mtorr, resulting in the crevices **4** formed at both sides in the respective grooves **3**. Incidentally, when the etching gas pressure is made to be higher than 500 mtorr, a dry etching speed is extremely decreased because of a degradation of the kinetic energy of the plasma gas itself.

Accordingly, it is preferable to employ an etching gas pressure range of 35 to 500 mtorr. Especially, in this range, it is possible to form the crevice **4** and the groove **3** having the dimensions shown in FIG. **10**.

According to the experimental results, the supporter 1B shown in FIG. **3** has been obtained under the conditions 1 to 3 described below.

Condition 1

etching gas: CF4

gas pressure: 35 mtorr

flow rate: 40 sccm

etching time 6 minutes and 5 second

Condition 2

etching gas: CF4

gas pressure: 50 mtorr

flow rate: 53 sccm

etching time 6 minutes and 25 second

Condition 3

etching gas: CF4

gas pressure: 65 mtorr

flow rate : 64 sccm

etching time 5 minutes and 55 second

According to this embodiment, the etching gas pressure used in the dry etching process in the present invention is 35 to 500 mtorr.

Under this condition, the grooves **3** and the crevices **4** are simultaneously formed or bored on the surface of the mirror supporter **1**.

In the above embodiments, the manufacture methods of the supporters **1A**, **1B** are explained in detail. Further, in the above embodiments, as the material of the mirror supporter **1**, the quartz glass and a soda lime glass are used, however, it is possible to employ soda alumina silicate glass or a barium borosilicate glass other than those glasses. Further, as the etching gas, CHF3 and CF4 are employed in the embodiments, however, it is not limited to those gases. It is possible to employ C2F6, C3F8, NF3, SF6 C2F4, C3F6, C4F8, C4F10, C5F8, C6F14, CF3CFOCF2, C6F5CF2CFCF2, CF3Br, CF31, C2F51, CF2Cl2, CFCl3 CH2F2, CHF2CF3, CH2FCF3, CH3CHF2, C2H3F3, C3HF7, CF3, CH2CF3, C6F5CHCH2, C12, CC14, SiCl4, BCl3, PCl3, CCl2F2, CCl3F, BBr3, CH2Cl2, CHCl3 and mixed gases thereof, and other mixed gases containing oxygen, hydrogen, argon, He, N2, Ne, Ar, Kr, Xe, O3, CO, CO2, H2O (vapor), CH4, CH3CH3, CH3CH2CH3, CH3CH2CH2CH3, CH2CH2, CH2CHCH3, CH2CH2CH2CH2, HCCH, and CH3CCH.

Further, in the above embodiments, the description is given of examples where glasses are used as the material of the supporter **1** and the supporter **1** is dry-etched. Needless to say, the material of the supporter **1** is not limited to glasses. Other materials such as a metal and a plastic resin may be employed, because a feature of the present invention resides in the surface shape formed or bored on the surface of the supporter **1**.

Accordingly, even when the supporter **1** is made of a plastic resin being shaped by using a stamper, it is applicable to the recording medium of the present invention as long as the supporter **1** has the same surface shape (lands, grooves and crevices) as mentioned in the foregoing.

The manufacturing method of such a stamper for producing a plurality of replicas of the supporter **1** is described in detail hereinafter. The manufacturing processes shown in FIGS. **15** (*a*) to (*e*) and **16** (*a*) to (*e*) are applied to a manufacture of a glass master having the same size as that of the supporter **1** or larger than that, and it is possible to produce the stamper as a replica of the glass master by using a conventional optical disc manufacturing process as it is.

Further, as mentioned in the foregoing, the manufacturing apparatus used for producing the supporter according to the manufacturing methods in the present invention may have means for forming a patterning mask on the supporter **1** which is polished in high precision and cleaned, means for forming a pattern on the supporter corresponding to a minute track pattern, means for simultaneously forming or boring the grooves and crevices in the supporter by a dry-etching method under a gas pressure of 35 to 500 mtorr and means for removing the patterning mask.

[Embodiment 3]

Next, a description is given of an information recording medium of a third embodiment in the present invention employing a plastic supporter as the supporter **1** and an improved DWDD layer as the recording layer.

FIGS. **19** (*a*) to **19** (*i*) are schematic view for explaining a third manufacturing method of the supporter in the present invention.

First, the description is given of a manufacturing method of a supporter of a third embodiment through an example of a plastic supporter having crevices, referring to FIGS. **19** (*a*) to **19** (*i*).

(1) preparing a base plate **11** (a diameter of 200 mm and a thickness of 10 mm) made of a soda lime glass being polished in high precise and cleaned (FIG. **19** (*a*)).

(2) forming a patterning mask **8** on the base plate **11** by coating a photo-resist as a masking material (FIG. **19** (*b*)).

(3) forming a pattern on the patterning mask **8** corresponding to a necessary minute track pattern by a conventional laser beam recording method (FIG. **19** (*c*)). Specifically, a spiral groove pattern was formed on the patterning mask **8** made of the photo-resist by irradiating and focusing the laser beam thereon with an objective lens, and was developed (not shown). Thereby, a parallel spiral pattern having flat portions **9** having a width of about 0.5 μm and opening portions **10** having a width of about 0.6 μm was obtained.

(4) Setting the base plate **11** in the parallel plate type dry etching apparatus BB (FIG. **18**), and dry etching the base plate **11** corresponding to the opening portions **10**

of the patterning mask **8** (FIG. **19** (*d*)). The dry etching conditions were as follows.

etching gas: CF4

gas pressure: 50 mtorr

flow rate: 53 sccm

etching time: 6 minutes 25 seconds

(5) removing the patterning mask **8** from the base plate **11** by an ashing treatment with oxygen plasma, resulting in a glass master **11B** (FIG. **19** (*e*)).

(6) forming a conductive layer **12** on the glass master **11B** by sputtering nickel at a thickness of 0.1 μm (FIG. **19** (*f*)).

(7) dipping the glass master **11B** in a nickel electroplating tab and causing the conductive layer **12** to grow to a plated layer **13** having a thickness of 250 μm by applying a voltage to the conductive layer **12** as a cathode (FIG. **19** (*g*)).

(8) integrally forming a stamper **14B** with the conductive layer **12** and the plated layer **13** by separating it from the glass master **11B** (FIG. **19** (*h*)).

(9) setting the stamper **14B** to an injection molding die after a bottom (having no pattern) of the stamper **14B** was polished and a periphery thereof was cut Then, a supporter **1B** having an upset pattern with respect to a concavity and a convexity was obtained by injection molding method using alicyclic polyolefin. The diameter of the supporter **1B** is 130 mm, and the thickness thereof is 1.2 mm (FIG. **19** (*i*)).

Further, the surface shape thereof satisfies the dimensions shown in FIG. **10**. Specifically, the width W1 of the land **2** is 0.51 μm and in the width (Wg+Wc) of the groove **3**, Wg is 0.51 μm, the depth Dg of the groove **3** is 0.2 μm and the width Wc of the crevice **4** is 0.04 μm and the depth Dc of the crevice **4** is 0.35 μm.

FIG. **20** is a section of other recording layer for explaining a concrete laminated structure of the recording layer in the present invention.

Next, on the supporter **1B**, there were formed the recording layer **5** and the protection layer **6**. The recording layer **5** was formed by the well known sputtering method using materials shown in FIG. **20**. Specifically, the recording layer **5** has a laminated construction by sandwiching an improved DWDD super-resolution layer 5 cl made of four magneto-optical layers (GdFeCoAl, TbFe, TbFeAl, and TbFeCo) between first and second SiN dielectric layers **5***d***1**, **5***d***2**. Next, the protection layer **6** was formed on the recording layer **5** at a thickness of 8 μm with an ultraviolet ray curing resin by the well known spin coating method, and was cured by irradiating an ultraviolet ray A+B+C wave.

This information recording disc was vertically cut to the track surface, and the section of the disc was observed with the scanning type electroscope. As a result, the section was confirmed to have the sectional shape shown in FIG. **4**.

FIG. **21** is a graph showing a mark length vs C/N reproduction frequency characteristic on a land recording of an information recording disc in the present invention, and

FIG. **22** is a graph showing a mark length vs C/N reproduction frequency characteristic on a groove recording of an information recording disc in the present invention.

Next, an information signal was recorded/reproduced on/from the information recording medium by irradiating and focusing a laser beam on the lands **2** thereof. As a result, a mark length vs C/N reproduction frequency characteristic was obtained as shown in FIG. **21**. In the recording apparatus used here, a laser beam having a wavelength of 690 nm and an objective lens having a numerical aperture of 0.6 were employed, and a single frequency recording/reproducing was carried out. The recording power was 3.7 mW and the reproducing power was 2.0 mW. At that time, it has been confirmed that the recording of a mark length of 0.06 μm was attained, resulting in a development of the super-resolution phenomenon. The C/N at a mark length of 0.1 μm was 36 dB which is enough for a practical use. Incidentally, the reproducing limitation obtained from a theoretical calculation using the wavelength and the numerical aperture is a mark length of 0.26 μm.

Next, the recording/reproducing was carried out by irradiating and focusing a laser beam on the groove **3** of the information recording disc, resulting in a mark length vs C/N reproducing frequency characteristics as shown in FIG. **22**. In this case, it was confirmed that the shortest mark length of 0.08 μm was attained, resulting in a development of the super-resolution phenomenon. The C/N at a mark length of 0.1 μm was 35 dB which is enough for a practical use.

As seen from FIGS. **21**, **22**, it was confirmed that the land/groove recording was attained even when the plastic supporter was employed as the supporter **1B**.

Next, the recording/reproducing of **1**, **7** modulation signal was carried out by focusing a laser beam on the land **2**. In the **1**, **7** modulation signal recording, signals having various kinds of mark lengths from 2T to 8T are recorded at random. When the shortest mark length (2T) was set to be 0.12 μm, the jitter of reproducing was 9.1%. This value of the jitter was enough for the practical use. Incidentally, the jitter was measured on the basis of Japanese Industrial Standard "120 mm DVD-Read-only disk" (JIS-X-6241: 1997 Annex F). The limitation of the reproduction obtained from a theoretical calculation using the wavelength and the numeral aperture is a mark length of 0.26 μm. Thus, it was confirmed that the super-resolution phenomenon was developed.

Next, a recording/reproducing was carried out in the same manner as mentioned above by focusing the laser beam on the groove **3**. When the shortest mark length (2T) was made to be 0.12 μm, the jitter of reproducing was 9.5%. This value of the jitter was enough for the practical use. As mentioned above, it has been confirmed that the land/groove recording was attained even when the random signal was employed.

[Embodiment 4]

Next, a description is given of an information medium of a fourth embodiment in the present invention, wherein a plastic supporter is employed as the supporter **1**, and a phase change recording layer is employed as the recording layer **5**. Further, in such a phase change recording layer as typically seen in the DVD-RAM where a land width is 0.74 μm and a groove width is 0.74 μm, thus, the track pitch is 1.48 μm, resulting in a recording capacity of 2.6 GB, the land/groove recording has been already put into practice. However, it was impossible to realize a larger recording capacity than that by decreasing the track pitch, because of a cross-erase phenomenon erasing adjacent tracks on recording.

On the other hand, according to the present invention, it is possible to decrease the track pitch by employ the supporter having crevices because of a decrease of the cross-erase phenomenon, resulting in a realization of a further higher recording density.

FIG. **23** is a chart showing concrete dimensions of the surface shape of the supporter in an embodiment of the present invention, and

FIG. **24** is a section of other recording layer for explaining a concrete laminated structure of the recording layer in the present invention.

Here, the plastic supporter **1B** is manufactured in the same manner as mentioned in the Embodiment 3, however, manu-

facturing conditions are slightly changed. The plastic supporter 1B is made of polycarbonate having a diameter of 120 mm and a thickness of 0.6 mm. Further, the surface shape thereof satisfies the dimensions shown in FIG. **23**. Specifically, the width W1 of the land **2** is 0.51 μm and in the width (Wg+2Wc) of the groove **3**, Wg is 0.51 μm, the depth Dg of the groove **3** is 0.06 μm and the width Wc of the crevice **4** is 0.04 μm and the depth Dc of the crevice **4** is 0.1 μm. Thus, a track pitch is 1.1 μm.

Next, on the supporter 1B, the recording layer **5** and the protection layer **6** were formed. The recording layer **5** was formed so as to have a structure shown in FIG. **24** by a well known sputtering method. Specifically, the recording layer **5** was formed by sandwiching a phase change recording layer **5***e***1** of GeSbTeN, which has the same construction as that of the DVD-RAM, between dielectric layers **5***f***1**, **5***f***2** of ZnS SiO. Further, a reflecting layer **5***g***1** of AlCr was formed on the dielectric layer **5***f***2**.

Next, as the protection layer **6**, an ultraviolet ray curing resin was coated at a thickness of 4 μm by a well known spray method, and cured by irradiating ultraviolet rays A+B wave. This information recording disc was vertically cut to the tracks, and the section of the disc was observed by using the scanning electron microscope, resulting in the sectional shape shown in FIG. **4**. Two sheets of these discs were adhered with an adhesive by causing the protection layers **6** thereof to face to each other (not shown). Further, as the adhesive layer formed therebetween, a slow curing cationic ultraviolet ray resin was used. Then, after initializing the information recording disc, an information signal was recorded/reproduced on/from the information recording disc.

The used recording apparatus had a laser beam having a wavelength of 650 nm, and an objective lens having a numeral aperture of 0.6. The recording power was 11 mW, the erasing power was 4.5 mW and the reproducing power was 1 mW. As the recording signal, **8–16** modulation random signal was used, wherein 3T as the shortest mark length was made to be 0.6 μm.

FIG. **25** is a chart showing measurement values of jitter on the land/groove recording of the information recording medium in the present invention.

First, continuously unrecorded three tracks were chosen, and the respective unrecorded tracks were named as a track a, track b and a track c. Then, an **8–16** random recording signal was recorded on the middle track b among them, and the recorded signal was successively reproduced from the track b and the jitter (J1) thereof was measured. Successively, the recording signal was recorded on the adjacent track a, and the jitter (J2) of the track b was measured. Further, the recording signal was recorded on the other adjacent track c, and the jitter (J3) of the track b was measured. These measurements of the jitter for the track b were repeated three times with respect to the land **2** and the groove **3**, respectively. The results are shown in FIG. **25**.

As the adjacent track of the track b is recorded, the value of jitter for the track b is increasing gradually, however, the increased value thereof is at most 0.6%, and the cross-erase was scarcely acknowledged. According to the 2.6 GB DVD-RAM Standard, a specific value of the jitter is determined to be not more than 8.5%. Thus, it will be understood that the values of jitter obtained from the experiments satisfy the specific values of the standard. This means that it is possible to shorten the track pitch from 1.48 to 1.1 μm, resulting in that the recording density of the information recording medium of this embodiment is increased 1.4 times as high as that of the conventional recording density.

[Comparative]

For comparison, the conventional disc shown in FIG. **6** was prepared, and the recording/reproducing characteristics thereof were measured in the same manner as mentioned in the foregoing. Here, the supporter **7** has the construction shown in FIG. **5**, and is made of polycarbonate. The width of the land **3** is made to be 0.51 μm and the width of groove **3** is made to be 0.59 μm. Thus, the track pitch thereof is made to be 1.1 μm which is the same as that of the embodiment 4.

FIG. **26** is a chart showing measurement values of jitter on the land/groove recording in the prior art.

The resultant measurement values of the jitter are shown in FIG. **26**. As seen from FIG. **26**, as the adjacent tracks are being recorded, the jitter of the middle track b is remarkably increasing, and shows a maximal increase amount of nearly 17%. In this case, a remarkable cross-erase has been developed. This means that it is impossible to shorten the track pitch when the conventional supporter is employed in the information recording medium.

As seen from the above description, the supporter having the crevices shows effective results in the jitter and the cross-erase problems even when it is employed for the phase change type recording disc. This reason is considered that the recording layer **5** is cut at every recording track by the crevice as shown in FIG. **4**. Thus, the crevices contributes to prevent heat which is generated by irradiating the laser beam on the adjacent recording tracks upon its recording, from transmitting to the corresponding track, resulting in a prevention of the cross-erase on the corresponding track.

In summary, according to the supporter used for an information recording medium in the present invention, lands and grooves are alternately formed as a minute track pattern on the supporter, and there is provided a crevice having a depth larger than that of the crevices in the respective grooves at one end thereof. Further, the information recording medium of the present invention is provided with a recording layer corresponding to a high density recording thereon, and the recording layer is cut at every recording track by the crevice. Thus, in the DWDD type super-resolution recording, it is possible to perform recording/reproducing without the laser annealing. This fact contributes to effectively produce such an information recording medium as having a high recording density in mass production.

Further, according to another supporter used for an information recording medium in the present invention, lands and grooves are alternately formed as a minute track pattern on the supporter, and there are provided two crevices in one groove, each having a depth larger than that of the respective grooves, at both ends of the respective grooves. Further, the information recording medium of the present invention has a recording layer corresponding to a high density recording thereon, and the recording layer is cut at every recording track by the crevice. Thus, it is possible to record an information recording signal without an reverse effect from the adjacent tracks, resulting in a realization of a further high density recording and a effective mass production of the information recording mediums.

Furthermore, according to a manufacture method of the supporter mentioned above, it is possible to produce the supporter in high precision.

Further, according to a manufacture apparatus and a stamper used for producing the supporter in the present invention, it is possible to simultaneously form or bore the grooves and the crevices in the supporter in high precision.

What is claimed is:

1. An information recording medium for recording an information signal thereon comprising:

a supporter on which lands and grooves are alternately formed as a minute track pattern, the lands and the grooves being flat and parallel to each other;

a crevice formed in the respective grooves on said supporter, the crevice having a sharp and pointed V-letter ditch extending to a depth larger than that of the respective grooves; and

a recording layer formed on the supporter except for said V-letter ditch of said crevice, such that said recording layer is divided into a plurality of spaced apart recording areas.

2. The information recording medium as claimed in claim 1, wherein the crevice is formed nearby an end of the respective grooves in a width direction of the respective grooves.

3. The information recording medium as claimed in claim 1, wherein the recording layer is cut at every track of the minute track pattern.

4. The information recording medium as claimed in claim 1, wherein the recording layer includes, at least, a magneto-optical layer with magnetic super resolution.

5. The information recording medium as claimed in claim 4, wherein the magneto-optical layer with magnetic super resolution is made of a domain wall displacement detection type information recording medium.

6. The information recording medium as claimed in claim 1 wherein the-recording layer includes, at least, a phase change recording layer.

7. An information recording medium for a recording information recording signal thereon comprising:

a supporter on which lands and grooves are alternately formed as a minute track pattern, the lands and the grooves being flat and parallel to each other;

two crevices formed in the respective grooves nearby both ends of the respective grooves in a width direction of the respective grooves on said supporter, with each of the two crevices having a sharp and pointed V-letter ditch extending to a depth larger than that of the respective grooves; and

a recording layer formed on the supporter except for said V-letter ditch of said crevices, such that the recording layer is divided into a plurality of spaced apart recording areas.

8. The information recording medium as claimed in claim 7, wherein the recording layer is cut at every track of the minute track pattern.

9. The information recording medium as claimed in claim 7, wherein the recording layer includes, at least, a magneto-optical layer with magnetic super resolution.

10. The information recording medium as claimed in claim 9, wherein the magneto-optical layer with magnetic super-resolution is made of a domain wall displacement detection type information recording medium.

11. The information recording medium as claimed in claim 7, wherein the recording layer includes, at least, a phase change recording layer.

12. A supporter used for forming a recording layer of an information recording medium thereof, wherein lands and grooves are alternately formed in the supporter as a minute track pattern, the lands and the grooves being flat and parallel to each other, and a crevice formed in the respective grooves having a sharp and pointed V-letter ditch extending to a depth larger than that of the respective grooves to cut the recording layer; and

a recording layer formed on the supporter except for each V-letter ditch in said crevices, such that the recording layer is divided into a plurality of spaced apart recording areas.

13. The supporter as claimed in claim 12, wherein the crevice is formed nearby an end of the respective grooves in a width direction of the respective grooves.

14. A supporter used for forming a recording layer of an information recording medium thereof, wherein lands and grooves are alternately formed in the supporter as a minute track pattern, the lands and the grooves being flat and parallel to each other, and two crevice each having a sharp and pointed V-letter ditch extending to a depth larger than that of the respective grooves formed in the respective grooves nearby both ends thereof in a width direction of the respective grooves to cut the recording layer;

a recording layer formed on the supporter except for said V-letter ditch of said crevices, such that the recording layer is divided into a plurality of spaced apart recording areas.

* * * * *

US005393406A

United States Patent [19]

Yokono et al.

[11] Patent Number: 5,393,406

[45] Date f Patent: Feb. 28, 1995

[54] **METHOD OF PRODUCING A THIN FILM MULTILAYER WIRING BOARD**

[75] Inventors: **Hitoshi Yokono**, Toride; **Hideo Arima**, Yokohama; **Takashi Inoue**, Yokohama; **Naoya Kitamura**, Yokohama, all of Japan

[73] Assignee: **Hitachi, Ltd.**, Tokyo, Japan

[21] Appl. No.: **845,942**

[22] Filed: **Mar. 4, 1992**

[30] **Foreign Application Priority Data**

Mar. 6, 1991 [JP] Japan 3-039833

[51] **Int. Cl.**[6] **C25D 5/02**

[52] **U.S. Cl.** **205/125**; 205/126

[58] **Field of Search** 205/125, 126; C25D 5/02; 29/846

[56] **References Cited**

U.S. PATENT DOCUMENTS

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Primary Examiner—John Niebling
Assistant Examiner—William T. Leader
Attorney, Agent, or Firm—Antonelli, Terry, Stout & Kraus

[57] **ABSTRACT**

A thin film multilayer wiring board-producing method of the present invention is intended to decrease thermal stresses developing during the formation of the multilayer construction, and also to greatly reduce the number of the steps of the process, as compared with a conventional method. A film material can be used as an insulating film of the multilayer wiring board, and is adhesively bonded to a predetermined portion. Wiring conductors are formed by electroplating. The wiring layers are repeated laminated to form the multilayer construction. A metallic film serving as an electrode is formed on one of upper and lower surfaces of a substrate, the metallic film being removed after a multilayer wiring is formed. A soluble insulating film is formed on a metallic undercoat film on the substrate, and grooves are formed in the soluble insulating film, and wiring conductors are formed in the grooves, using either electroplating or both electroplating and electroless plating. Thereafter, the soluble insulating film and the metallic undercoat film are removed. Subsequently, an insoluble insulating film is formed at those locations from which the soluble insulating film and the metallic undercoat have been removed.

2 Claims, 11 Drawing Sheets

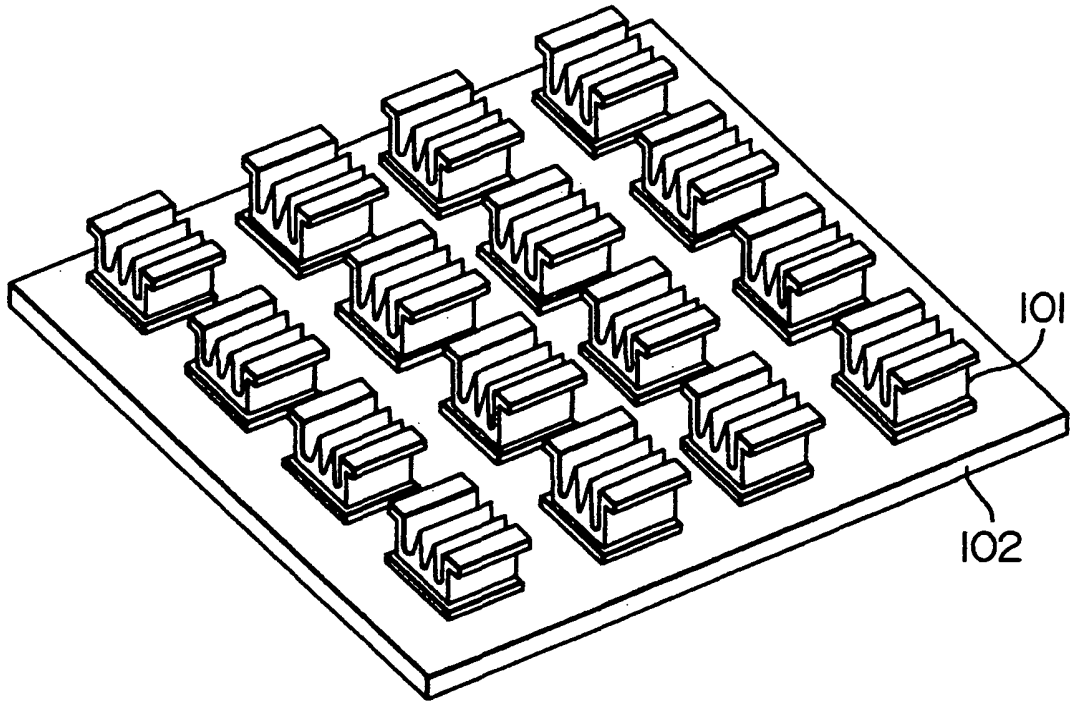


FIG. 1A
PRIOR ART

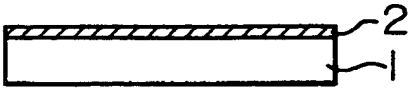


FIG. 1B
PRIOR ART

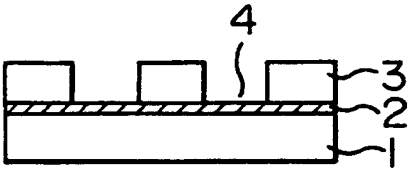


FIG. 1C
PRIOR ART

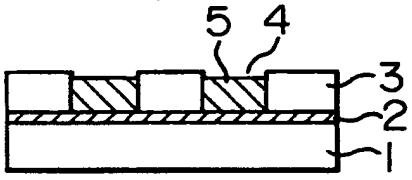


FIG. 1D
PRIOR ART

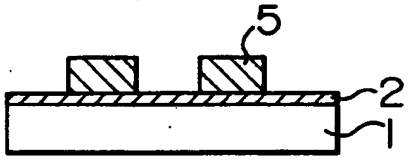


FIG. 1E
PRIOR ART

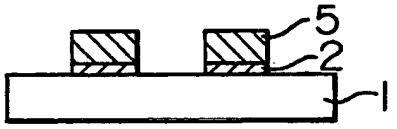


FIG. 1F
PRIOR ART

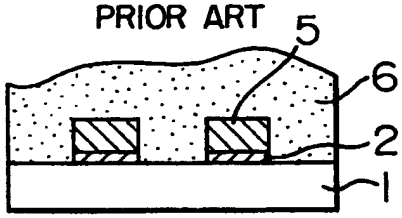


FIG. 1G
PRIOR ART

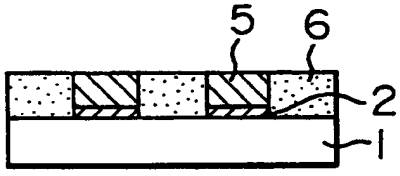


FIG. 2

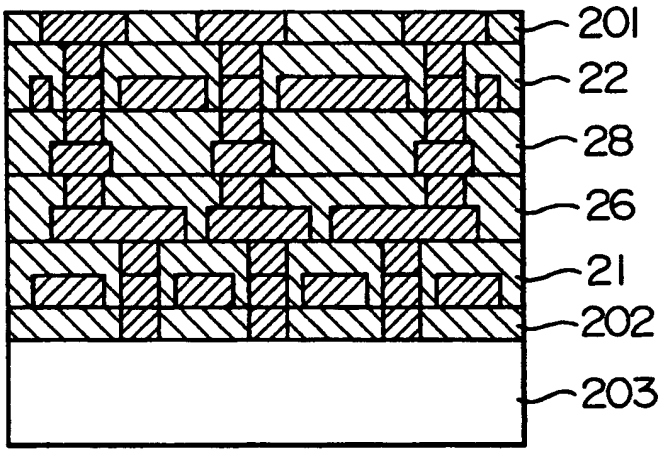


FIG. 3

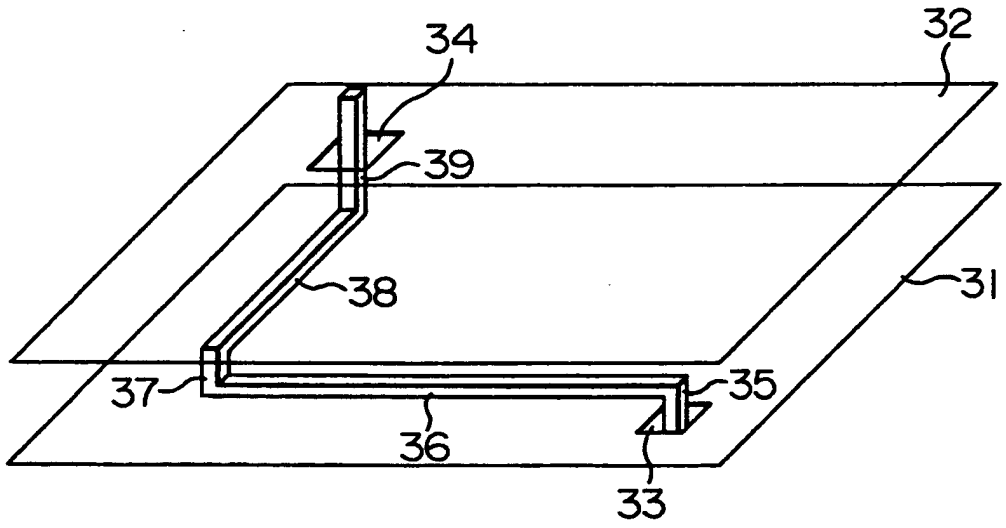


FIG. 4A

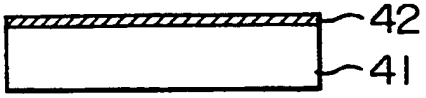


FIG. 4B

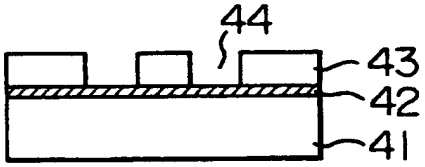


FIG. 4C

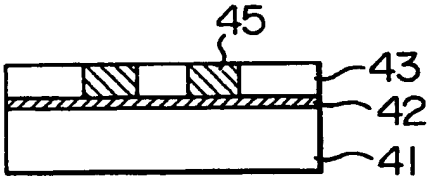


FIG. 4D

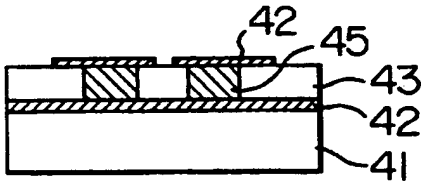


FIG. 4E

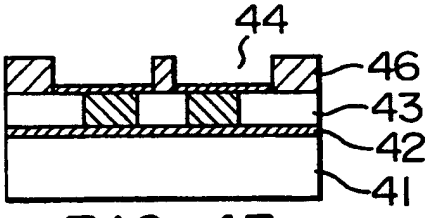


FIG. 4F

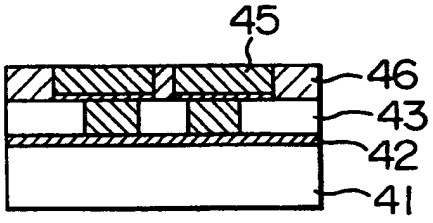


FIG. 4G

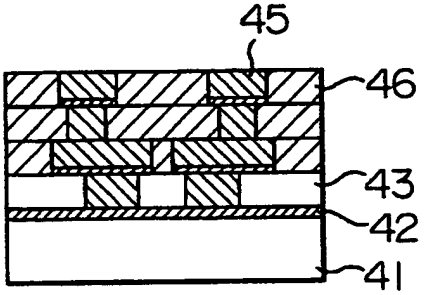


FIG. 4H

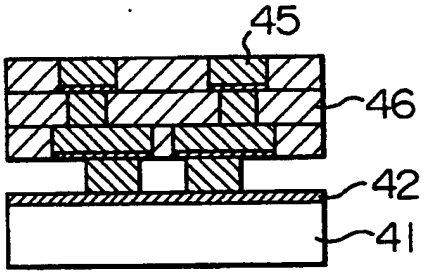


FIG. 4I

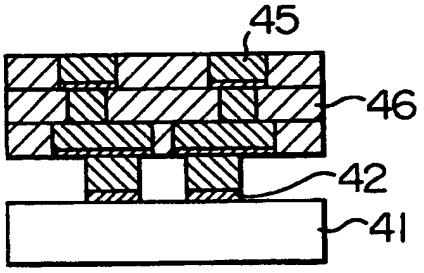


FIG. 4J

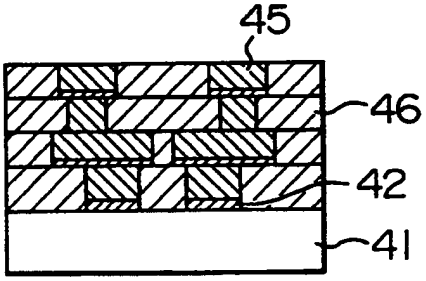


FIG. 5A

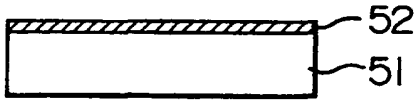


FIG. 5B

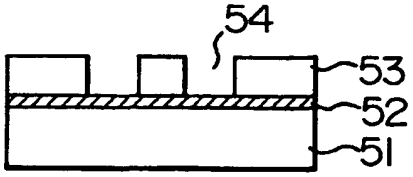


FIG. 5C

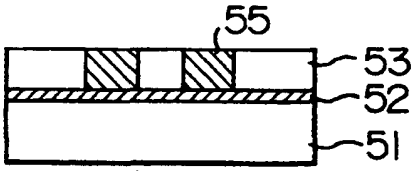


FIG. 5D

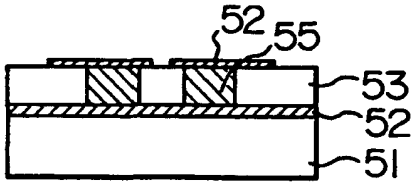


FIG. 5E

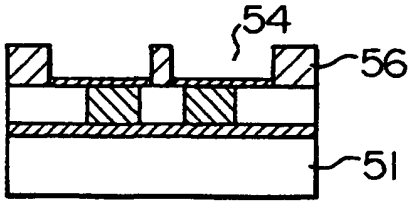


FIG. 5F

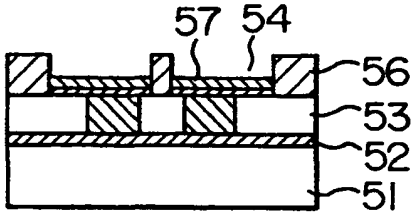


FIG. 5G

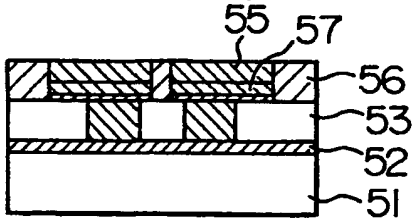


FIG. 5H

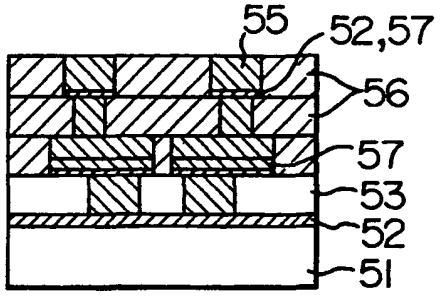


FIG. 5I

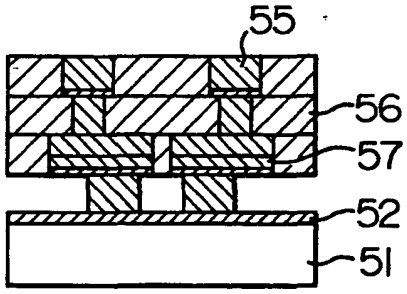


FIG. 5J

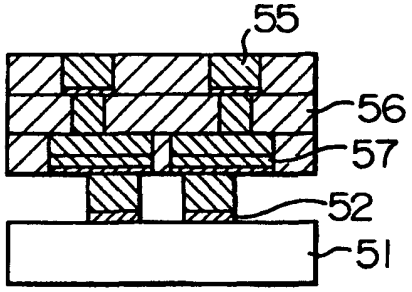


FIG. 5K

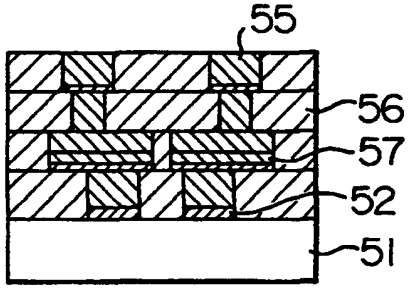


FIG. 6A

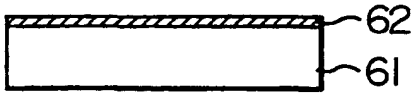


FIG. 6B

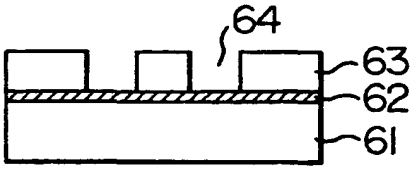


FIG. 6C

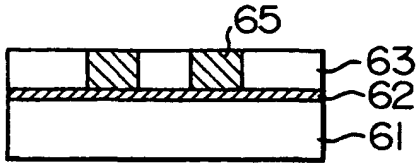


FIG. 6D

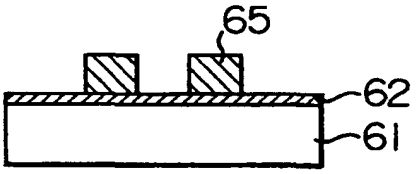


FIG. 6E

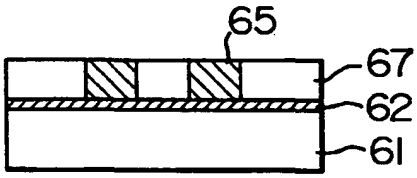


FIG. 6F

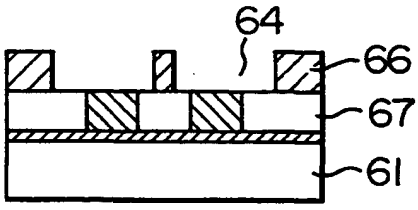


FIG. 6G

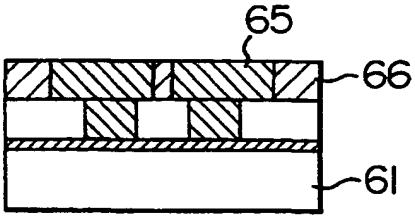


FIG. 6H

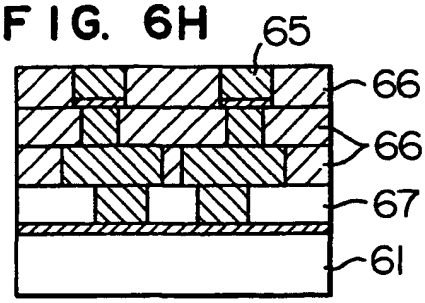


FIG. 6I

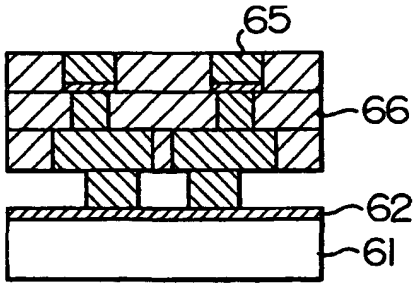


FIG. 6J

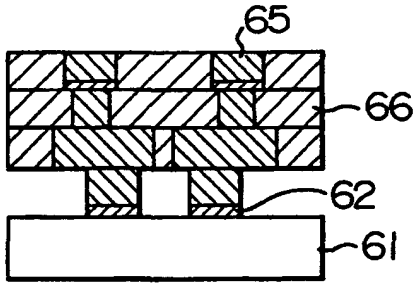


FIG. 6K

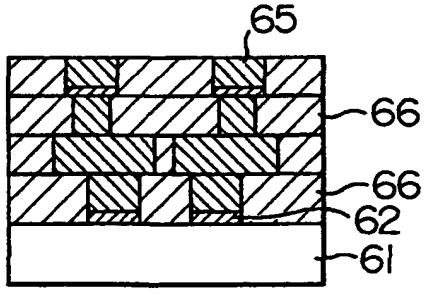


FIG. 7A

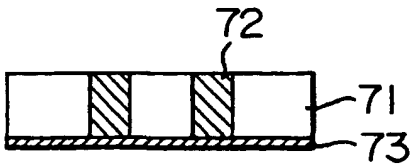


FIG. 7B

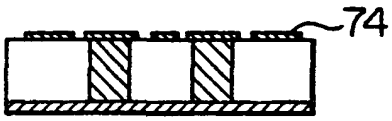


FIG. 7C

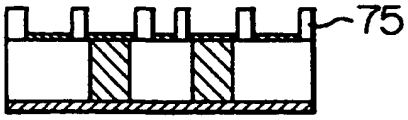


FIG. 7D

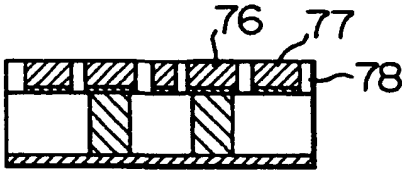


FIG. 7E

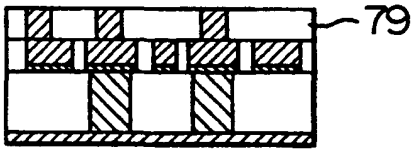


FIG. 7F

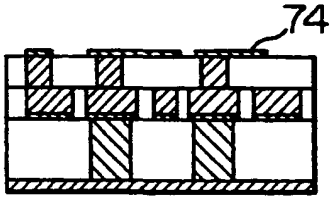


FIG. 7G

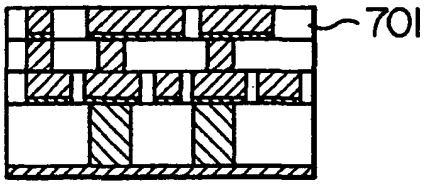


FIG. 7H

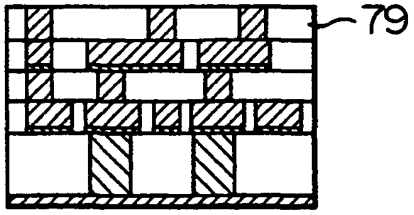


FIG. 7I

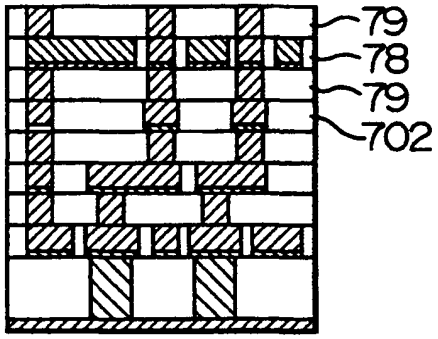


FIG. 7J

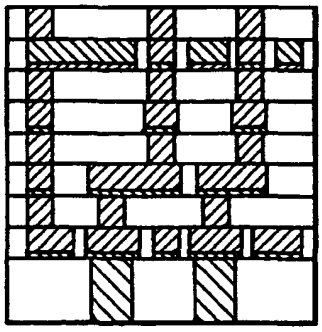


FIG. 8

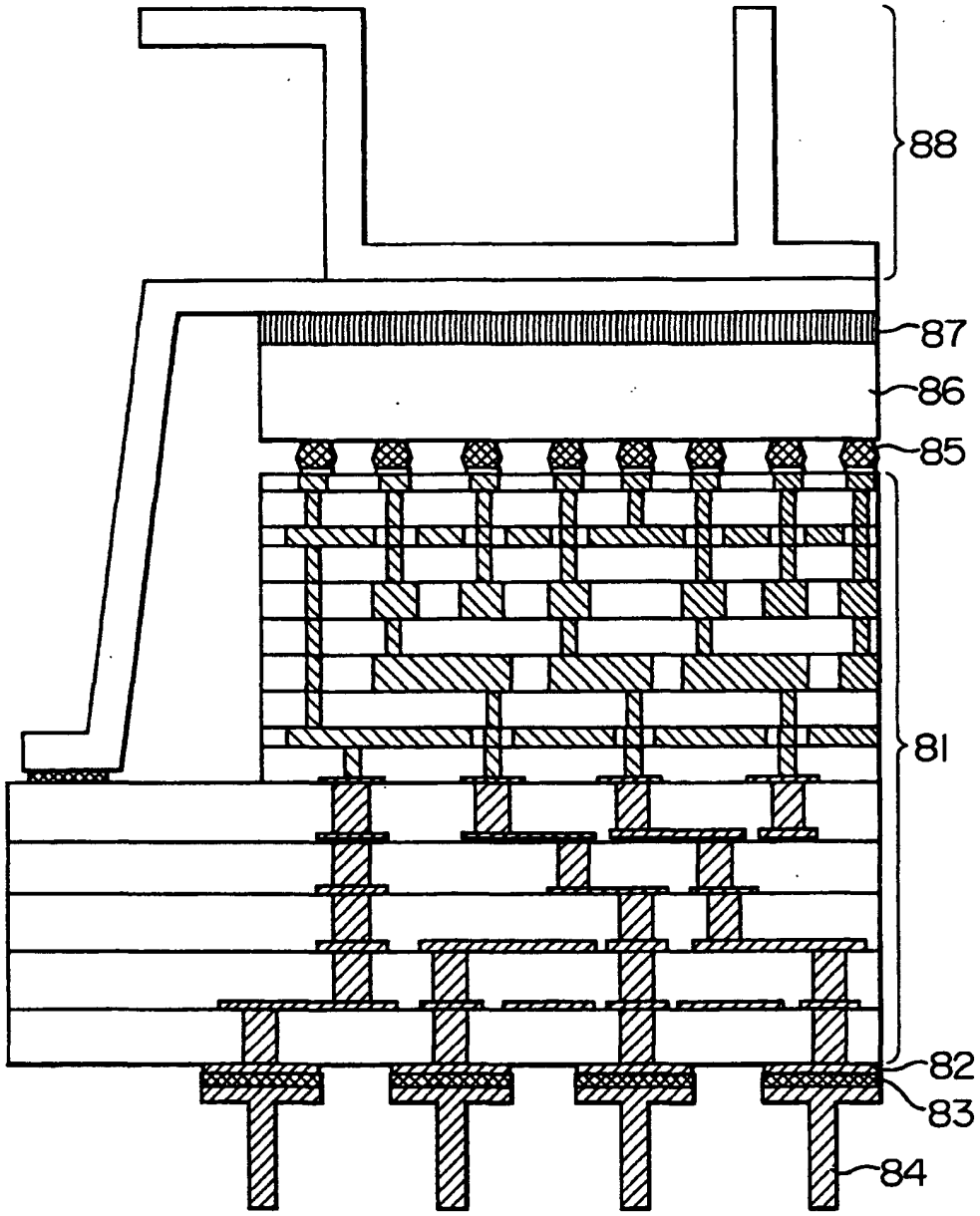


FIG. 9

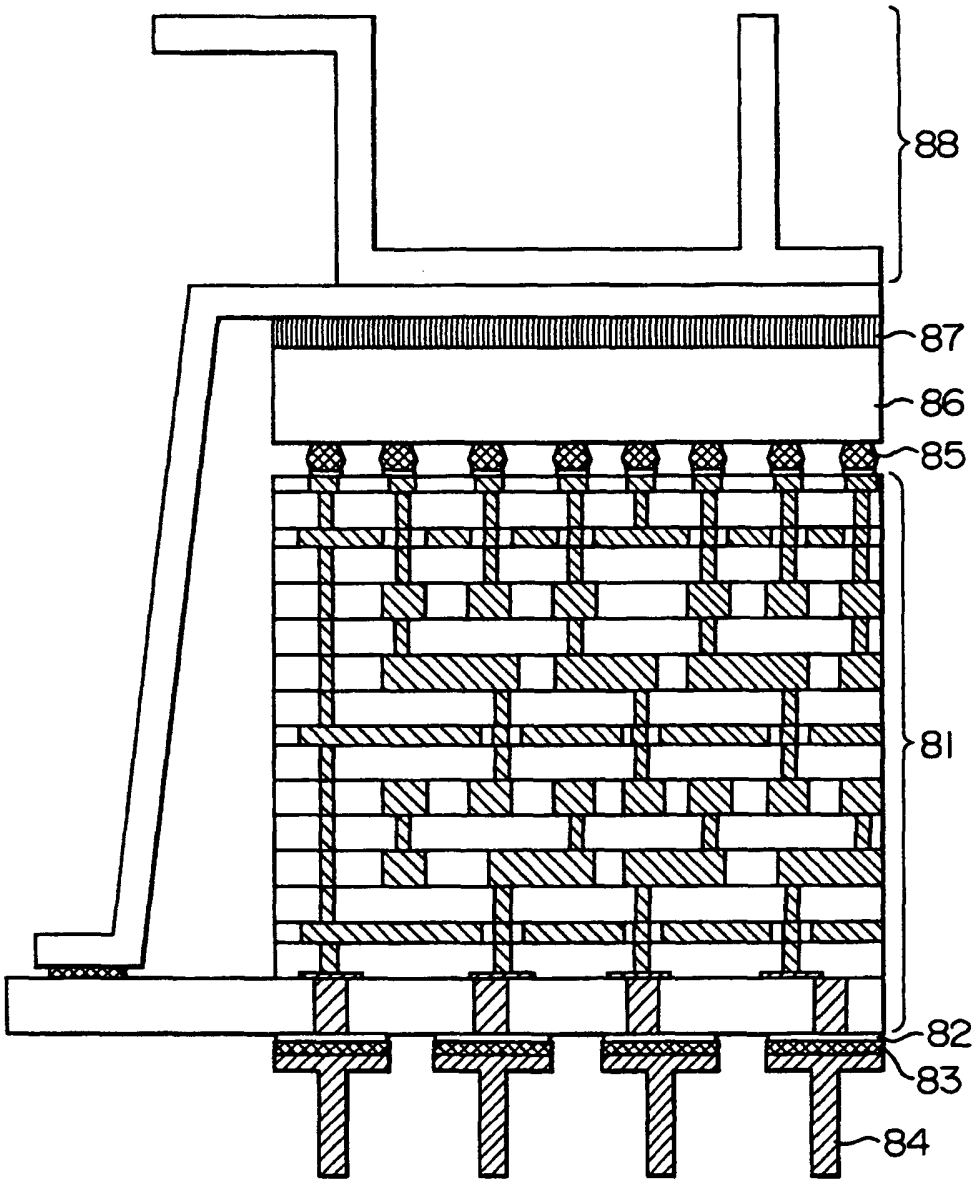
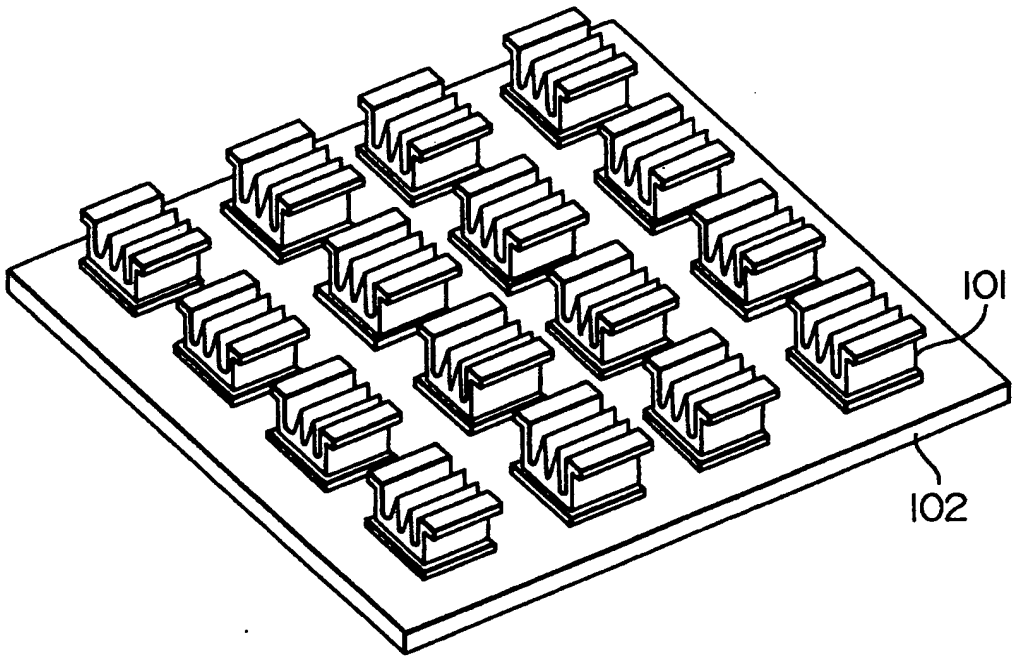


FIG. 10



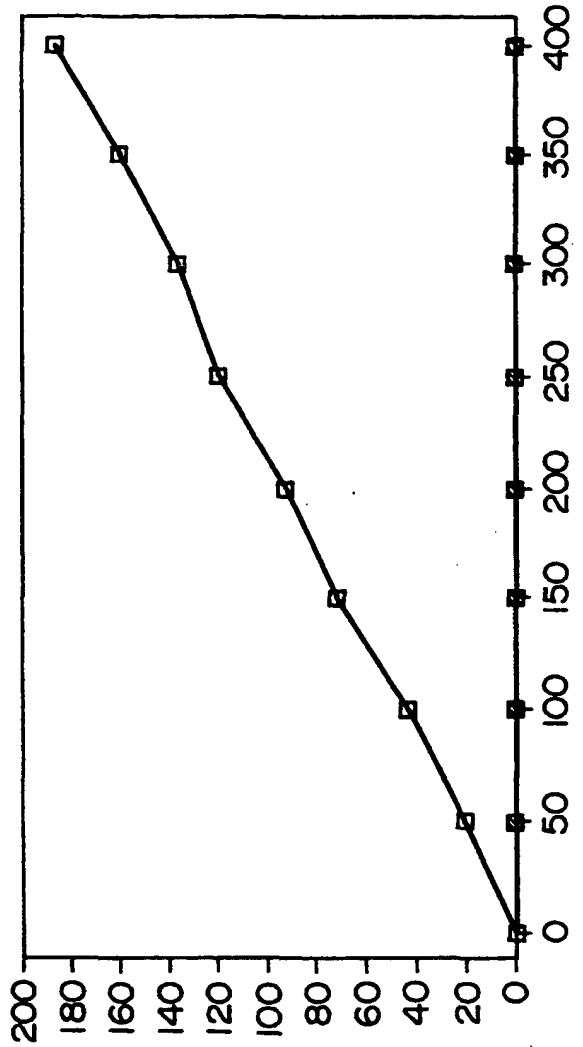


FIG. 11A

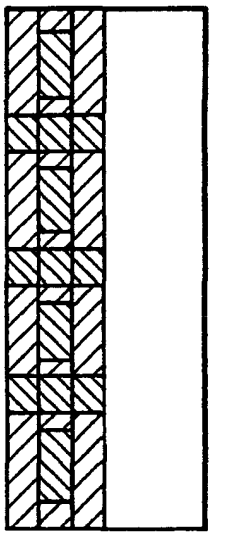


FIG. 11C

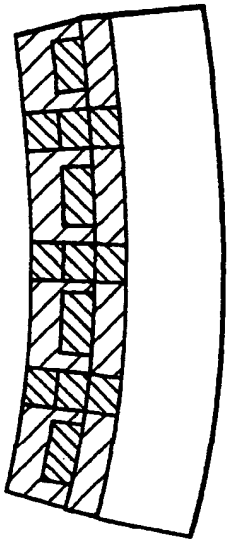


FIG. 11B

METHOD OF PRODUCING A THIN FILM MULTILAYER WIRING BOARD

FIELD OF THE INVENTION

This invention relates to a thin film multilayer wiring board for densely packaging highly-integrated LSIs, terminal resistors, capacitors and so on, and also relates to a method of producing such a wiring board, with the thin film multilayer wiring board being adapted to be used for a module, and is used as a wiring board of a computer.

BACKGROUND OF THE INVENTION

A typical conventional method of producing a thin film multilayer wiring board will be described with reference to steps (a) to (g) of the method as shown in FIGS. 1A-1C.

In the step (a), a metallic undercoat film 2 is formed on an upper surface of a substrate 1. This metallic undercoat film 2 is used as a plating electrode at a later stage.

In the step (b), a resist layer 3 is formed, and this layer is grooved into a configuration corresponding to a predetermined conductor pattern.

In the step (c), a conductor is filled in grooves 4 in the resist layer 3 by electroplating, thereby forming conductors 5 such as horizontally-extending wiring conductors, via hole conductors, through hole conductors and ground layer conductors.

In the step (d), the resist layer 3 is removed to expose the conductors 5.

In the step (e), the metallic undercoat film 2, except for those portions thereof disposed immediately beneath the conductors 5, is removed by etching.

In the step (f), an insoluble insulating layer 6 is formed on the upper surface of the substrate 1 so as to cover the conductors 5.

In the step (g), the insoluble insulating layer 6 is ground and polished so as to expose the upper surfaces of the conductors 5 and also to flatten the upper surface of the insoluble insulating layer 6.

With these steps (a) to (g), a thin film single-layer wiring board is formed, and then these steps (a) to (g) are repeated several times to form a thin film multilayer wiring board.

This conventional method is described in "Thin-film Conductors and Conductor Processes" on pages 710 to 714 (Item 9.6.2) of Microelectronics Packaging, edited by Rao R, Tummala and Eugene J. Rymaszewski, VAN NOSTRAND REINHOLD, and is described in detail particularly in FIGS. 9-21 on page 713.

In the above conventional method, however, when a thin film multilayer wiring board is to be produced, it is necessary to carry out the steps (a) to (g) illustrated in FIGS. 1A to 1G for forming each of the layers of the multilayer wiring board, and therefore the number of the steps involved is very large. Particularly, in the step (f), the insoluble insulating layer 6 is formed on the rugged portion defined by the substrate 1 and the conductors 5, and therefore the insoluble insulating layer 6 thus formed also becomes rugged. As a result, the step (g) of grinding and polishing the insoluble insulating layer 6 so as to flatten this layer is essential.

As later described, as the insoluble insulating layer, a polymeric material, such as polyimide, polyamide, polyamide-imide, polyester and polycarbonate may be employed. These materials become softened and viscous due to a temperature rise during the grinding and polishing operation, which results in a problem that the grinding and polishing are difficult and take much time. Another problem is that when the via conductors and so on are ground simultaneously with the grinding of the insoluble insulating layer, metal powder resulting therefrom is scattered, and adheres to the softened polymeric material. The metal powder may not be easily removed from the polymeric material by washing.

Therefore, there is a possibility that contaminants, such as powder of the polymer, may be present in each layer of the thin film multilayer wiring board. Therefore, in order to enhance the reliability, the step of washing away the contanimants, as well as the step of inspecting an electrical defect, are needed in addition to the above steps (a) to (g). Moreover, when an electrically-defective product (the thin film multilayer wiring board having a defect at least in one layer thereof) is found in this inspection step, an additional step must be carried out in order to reuse such an electrically-defective product, and it is practically difficult to remove the several μm-thick thin film layer at the defective portion. Consequently, a considerable number of defective products have been produced, and the yield rate was inevitably low.

Further, in the thin film multilayer wiring board produced by the above method, the insoluble insulating layer 6 is coated on the rugged portion defined by the substrate 1 and the conductors 5, and therefore a liquid material must be used for forming the insoluble insulating layer 6. When the liquid material is to be cured or set into a solid by a heat treatment, stresses of different values develop due to a large difference in thermal expansion coefficient between the substrate 1, the metallic undercoat film 2, the conductors 5 and etc. These stresses have caused warping of the thin film multilayer wiring board.

As described above, the above conventional method of producing the thin film multilayer wiring board suffers from the problems with the mass productivity, the reliability and the yield rate, and besides there is encountered another problem that warping is present in the resultant thin film multilayer wiring board.

SUMMARY OF THE INVENTION

With the above problems of the prior art (that is, a low mass-productivity due to an increased number of the process steps, a low reliability and a low yield rate due to the generation of contaminants during the grinding and polishing operation) in view, it is an object of this invention to provide a method of producing a thin film multilayer wiring board which is excellent in mass-productivity, reliability and yield rate.

With the warp problem of the prior art in view, it is another object of the invention to provide a thin film multilayer wiring board which is less warped.

A thin film multilayer wiring board-producing method of the present invention is performed by the following processes (A) to (C). With respect to the formation of each layer, the grinding and polishing for flattening an insoluble insulating film are not necessary, and also the formation and removal of a resist is not necessary except for the first layer. Further, the removal of a metallic undercoat film is not necessary except for the first layer. Therefore, the mass productivity, the reliability and the yield are excellent.

(A) A thin film multilayer wiring board-producing method is characterized by the steps f:

(1) forming a first metallic undercoat film on a substrate, then forming a soluble insulating film on the metallic undercoat film, and forming grooves in the soluble insulating film, and then filling a conductor in the grooves by electroplating, thereby forming a first layer;

(2) subsequently forming an insoluble insulating film on the first layer or on a horizontal metallic undercoat film formed on the first layer, and forming grooves in the insoluble insulating film, and then filling a conductor in the grooves by the use of electroplating or both electroless plating and electroplating, thereby forming a second layer on the first layer; and

(3) subsequently removing the soluble insulating film and the first metallic undercoat film, and forming an insoluble insulating film at those portions from which the soluble insulating film and the first metallic undercoat film have been removed.

(B) A thin film multilayer wiring board-producing method is characterized by the steps of:

(1) forming a first metallic undercoat film on a substrate, then forming a soluble insulating film on this metallic undercoat film, and forming grooves in the soluble insulating film, then filling a conductor in the grooves by electroplating, then removing the soluble insulating film, and then forming a metallic film, capable of selective etching with respect to the conductor, at that portion from which the soluble insulating film has been removed, thereby forming a first layer;

(2) subsequently forming an insoluble insulating film on the first layer or on a horizontal metallic undercoat film formed on the first layer, and forming grooves in the insoluble insulating film, and then filling a conductor in the grooves by the use of electroplating or both electroless plating and electroplating, thereby forming a second layer on the first layer; and

(3) subsequently removing the metallic film, capable of selective etching with respect to the conductor, and the first metallic undercoat film, and then forming an insoluble insulating film at those portions from which the metallic film and the first metallic undercoat film have been removed.

(C) A thin film multilayer wiring board-producing method is characterized by the steps of:

(1) forming a first metallic film on a lower surface of a substrate, and forming an insoluble insulating film on an upper surface of the substrate or on a horizontal metallic undercoat film formed on the upper surface of the substrate, then forming grooves in the insoluble insulating film, and then filling a conductor in the grooves by the use of electroplating or both electroless plating and electroplating, thereby forming a first layer on the upper side of the substrate;

(2) subsequently forming an insoluble insulating film on the first layer or on a horizontal metallic undercoat film formed on the first layer, and forming grooves in the insoluble insulating film, and then filling a conductor in the grooves by the use of electroplating r both electroless plating and electroplating, thereby forming a second layer on the first layer;

(3) subsequently rem ving the first metallic film.

One preferred form of the thin film multilayer wiring board of the present invention is described in Item (D) bel w. A liquid material is beforehand cured by a heat treatment into a solid form to provide a film material, and this film material is used as an insoluble insulating film. Therefore, no undesirable stresses of different values will develop due to a large difference in thermal expansion coefficient between a substrate, a metallic undercoat film and conductors. As a result, the thin film multilayer wiring board extremely reduced in warp can be obtained.

(D) A thin film wiring board comprising one or more layers formed on a substrate, with each of the layers comprising a conductor, an insoluble insulating film, and optionally a metallic undercoat film provided beneath the conductor, and the insoluble insulating film being an insoluble film material adhesively bonded.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A–1G are cross-sectional views showing a sequence of steps of a conventional method of producing a thin film multilayer wiring board;

FIG. 2 is a cross-sectional view showing one set of signal layers;

FIG. 3 is a schematic and perspective view showing a basic construction of a wiring conductor;

FIGS. 4A–4J are cross-sectional views of the sequence of steps of a method of producing a thin film multilayer wiring board according to the present invention;

FIGS. 5A–5K are cross-sectional views of a sequence of steps of a modified method of producing a thin film multilayer wiring board according to the present invention;

FIGS. 6A–6K are cross-sectional views showing the sequence of steps of another modified method of producing a thin film multilayer wiring board according to the present invention;

FIGS. 7A–7J are cross-sectional views showing the sequence of steps of a further modified method of producing a thin film multilayer wiring board according to the present invention;

FIG. 8 is a cross-sectional view of a module using thick and thin film multilayer wiring boards of the invention;

FIG. 9 is a cross-sectional view of a module using thin film multilayer wiring boards of the invention;

FIG. 10 is a perspective view of a logic package of a computer, provided in accordance with the present invention; and

FIG. 11 is an illustration showing the relation between a polyimide film thickness and a warp of a substrate.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The inventors of the present invention have made an extensive study, noting that in the above-mentioned conventional method of producing the thin film multilayer wiring board, particularly since in the step (f), the insoluble insulating film 6 is formed on the rugged portion defined by the substrate and the conductors 5 with the result that the insoluble insulating film 6 thus formed is rugged, the step (g) of grinding and polishing the insoluble insulating layer 6 to flatten the same is essential, and that this extremely lowers the mass-productivity, the reliability and the yield rate. As a result of the extensive study, the inventors f the present invention

have noted that by forming an insulating film on a flat portion, the insulating film thus f rmed is also flat, and based on this finding, the inventors have found a method of producing a thin film multilayer wiring board according to the present invention. A thin film multilayer wiring board is produced by any one of the following methods (A) to (C) of the present invention. To further increase the number of the layers, in the method (A), the step (A)(2) is further repeated one or more times. Similarly, in the method (B), the step (B)(2) is further repeated one or more times. Similarly, in the method (C), the step (C)(2) is further repeated one or more times. With the methods (A) to (C), the grinding and polishing for flattening the insoluble insulating film become unnecessary with respect to the formation of any layer, and besides the formation and removal of a resist become unnecessary with respect to the formation of other layers than the first layer, and further the removal of a metallic undercoat film becomes unnecessary with respect to the formation of other layers than the first layer. Therefore, the mass-productivity, the reliability and the yield rate are excellent.

(A) A thin film multilayer wiring board-producing method is characterized by the steps of:

(1) forming a first metallic undercoat film on a substrate, then forming a soluble insulating film on the metallic undercoat film, and forming grooves in the soluble insulating film, and then filling a conductor in the grooves by electroplating, thereby forming a first layer;

(2) subsequently forming an insoluble insulating film on the first layer or on a horizontal metallic undercoat film formed on the first layer, and forming grooves the insoluble insulating film, and then filling a conductor in the grooves by the use of electroplating or both electroless plating and electroplating, thereby forming a second layer on the first layer; and

(3) subsequently removing the soluble insulating film and the first metallic undercoat film, and forming an insoluble insulating film at those portions from which the soluble insulating film and the first metallic undercoat film have been removed. (B) A thin film multilayer wiring board-producing method is characterized by the steps of:

(1) forming a first metallic undercoat film on a substrate, then forming a soluble insulating film on this metallic undercoat film, and forming grooves in the soluble insulating film, then filling a conductor in the grooves by electroplating, then removing the soluble insulating film, and then forming a metallic film, capable of selective etching with respect to the conductor, at that portion from which the soluble insulating film has been removed, thereby forming a first layer;

(2) subsequently forming an insoluble insulating film on the first layer or on a horizontal metallic undercoat film formed on the first layer, and forming grooves in the insoluble insulating film, and then filling a conductor in the grooves by the use of electroplating or both electroless plating and electroplating, thereby forming a second layer on the first layer; and

(3) subsequently removing the metallic film, capable of selective etching with respect to the conductor, and the first metallic undercoat film, and then forming an insoluble insulating film at those portions from which the metallic film and the first metallic undercoat film have been removed.

(C) A thin film multilayer wiring board-producing method is characterized by the steps of:

(1) forming a first metallic film on a lower surface of a substrate, and forming an insoluble insulating film on an upper surface of the substrate or on a horizontal metallic undercoat film formed on the upper surface of the substrate, then forming grooves in the insoluble insulating film, and then filling a conductor in the grooves by the use of electroplating or both electroless plating and electroplating, thereby forming a first layer on the upper side of the substrate;

(2) subsequently forming an insoluble insulating film on the first layer or on a horizontal metallic undercoat film formed on the first layer, and forming grooves in the insoluble insulating film, and then filling a conductor in the grooves by the use of electroplating or both electroless plating and electroplating, thereby forming a second layer on the first layer;

(3) subsequently removing the first metallic film.

In the thin film multilayer wiring board produced by the above conventional method, the insoluble insulating layer 6 is formed on the rugged portion defined by the substrate 1 and the conductors 5, and therefore a liquid material must be used for forming the insoluble insulating film 6. When the liquid material is to be cured or set into a solid by a heat treatment, stresses of different values develop due to a large difference in thermal expansion coefficient between the substrate 1, the metallic undercoat film 2, the conductors 5 and etc. This has resulted in a warp of the thin film multilayer wiring board. The inventors of the present invention have noted this point, and have made an extensive study, and have found that such a liquid material does not need to be used to form the insulating film on the flat portion, and that a film-like insulating material (film-like material) can be used. Based on this finding, the inventors of the present invention have invented the thin film multilayer wiring board of the present invention. The thin film multilayer wiring board of the present invention has any one of the following constructions (D) to (F). With such construction of the present invention, a liquid material does not need to be used for forming the insulating film with respect to the formation of all layers, and a film-like insulating material to be adhesively bonded can be used. Therefore, there can be obtained the thin film multilayer wiring board subjected to less warp.

(D) A thin film wiring board comprising one or more layers formed on a substrate, each of the layers comprising a conductor, an insoluble insulating film, and optionally a metallic undercoat film provided beneath the conductor, and the insoluble insulating film being an insoluble film material adhesively bonded.

(E) A thin film wiring board as defined in the above Item (D) wherein the film material consists of at least one selected from the group consisting of a polyimide film, a polyamide film, a polyamide-imide film, a polyester film and a polycarbonate film.

(F) A thin film wiring board as defined in the above Item (D) wherein the metallic undercoat film consists of at least one material selected from the group consisting of Cr, Cu, Ti, Zn, Sn, Co, Fe, Ni, Rh and In.

Next, the above methods (A) to (C) of producing the thin film multilayer wiring board according to the pres-

ent invention, as well as the above constructions (D) to (F), will be described in detail.

In the conventional thin film multilayer wiring board-producing method, one major reason why the formation and removal of the photoresist are carried out with respect to each layer is that the metallic undercoat film serving as the electrode of the electroplating must be formed and removed with respect to each layer. Therefore, first, attention was directed to the steps of formation and removal of the metallic undercoat film serving as the electrode of the electroplating, and an attempt has been made to rationalize these two steps in order to rationalize the steps of formation and removal of the photoresist.

If the wiring conductors of the thin film multilayer wiring board are constituted only by through hole conductors extending from the uppermost layer to the lowermost layer, the lengths of all the through hole conductors are the same, and those portions at the same level or height are at the same electrical potential when carrying out the electroplating. Therefore, in this case, it is necessary to provide the metallic undercoat film only at the lowermost layer, and there is no need to provide it at all of the layers.

Actually, however, the wirings, provided in the interior of the thin film multilayer wiring board, include not only the through hole conductors of the same length, but also horizontally-extending X-direction and Y-direction wirings as well as ground layer conductors electrically interrupted from via hole conductors, as shown in FIG. 3. In order to form these conductors by electroplating, it is necessary to provide the metallic undercoat film (serving as the electrode) under each of them. This is the reason why the metallic undercoat film must be provided at each layer in the conventional thin film multilayer wiring board.

Although its internal structure may be slightly varied or modified, a thin film multilayer wiring board can be produced by repeatedly forming this one set of signal layers. One set of signal layers of FIG. 2 comprises a surface layer 201, an upper ground layer 22, an X-direction wiring 28, a Y-direction wiring 26, a lower ground layer 21, a matching layer 202, and a thick film substrate 203. The wiring conductors of the upper ground layer 22, the X-direction wiring 28, the Y-direction wiring 26 and the lower ground layer 21 will be described in detail with reference to FIG. 3. A via or through-hole wiring 35, electrically interrupted from the lower ground layer 31, is disposed at the lowermost ground layer 31, and extends through a hole 33 formed through the lower ground layer 31, and a horizontally-extending Y-direction wiring 36 is disposed at the upper layer adjacent thereto, and a via wiring 37 extends upwardly from the Y-direction wiring 36 to a horizontally-extending X-direction wiring 38, and a via or through-hole wiring 39, extends upwardly from the X-direction wiring 38. The wiring 39 extends through a hole 34 formed through the upper ground layer 32 from which the wiring 39 is electrically interrupted.

When an LSI and a power source are not connected to the thin film multilayer wiring board, the wiring conductors provided in the interior of this wiring board are not electrically connected to one another, and are independent of one another. Therefore, in order that the wiring conductors at each layer can be formed at a time by electroplating, the metallic undercoat film serving as the electrode must be provided ver the entire area of the substrate, because any portions of this layer need to have the same potential. After the formati n of the conductors, the wirings must be electrically interrupted from one another, and therefore the metallic undercoat film except for those portions thereof disposed immediately beneath the wiring conductors must be removed by etching. In order to remove the metallic undercoat film by etching, it is necessary to remove the photoresist covering it. This is the reason why in the formation of the wiring conductors in the conventional method, instead of an insulating film which can not be easily removed by dissolving, the photoresist which can be removed by dissolving is used as the polymer in which the grooves are formed so as to form the wiring conductors by electroplating.

In the present invention, as shown in FIG. 2, a photoresist is not used as the polymer in which the grooves are formed so as to form the wiring conductors, and instead the permanent insulating film is used. Therefore, the step of forming the photoresist and the step of removing it are omitted. This means that the removal of the metallic undercoat film by etching after the removal of the photoresist is also unnecessary except for the metallic undercoat film of the lowermost layer over the entire surface of the substrate.

However, this does not means that the metallic undercoat film is unnecessary except for the lowermost layer, and so long as the wiring conductors are formed by electroplating, the metallic undercoat film is still necessary to provide the electrodes disposed immediately beneath the X-direction and Y-direction wiring conductors and the ground layer conductor. Thus, it is to be noted that it is not necessary to form the metallic undercoat film over the entire area of the substrate in such a manner as to extend between the wiring conductors.

When the metallic undercoat film is to be formed over the entire surface of the substrate by electroplating, the only requirement to be satisfied is that the metallic undercoat film should have the same potential at any portion of the substrate, and therefore usually, the metallic undercoat film is formed into a thickness of not more than 1 μm. In the present invention, however, as the metallic undercoat film for the X-direction and Y-direction wiring conductors is away from the metallic undercoat film of the lowermost layer, the electrical resistivity of the metallic undercoat film to be disposed immediately beneath the X-direction and Y-direction wiring conductors increases. Therefore, the height of the conductor precipitated by electroplating becomes gradually smaller, which results in a problem that a large difference in height between both ends of the wiring conductor develops. In view of this, in the present invention, in order to decrease the electrical resistivity of the metallic undercoat film formed in accordance of the areas of the lower surfaces of the X-direction and Y-direction wiring conductors, the film thickness is increased. One means for achieving this is to increase the thickness of the metallic undercoat film from the beginning. Another means is to first form a metallic undercoat film of not more than 1 μm thickness in the conventional manner and then to increase its thickness by electroless plating.

Preferably, variations in the height of the wiring conductor should be not more than 10%. To meet this requirement, the inventors of th present invention have confirmed through experiments that the resistivity of the metallic undercoat film (disposed immediately beneath the X-direction and Y-direction wiring conduc-

tors) between both ends f the wiring sh uld be less than several tens of Ω. For example, if the metallic undercoat film of copper has a thickness of 1 μm, a width of 30 μm and a length of 200 mm, the resistivity of this metallic undercoat film is about 110 Ω. Then, as shown in FIGS. 4A–4J, when by electroless plating, copper is precipitated about 1 to 5 μm in the groove formed in the insulating film (20 μm in width) formed on this metallic undercoat film, the resistivity is reduced to 70 to 26 Ω and variations in the thickness of the wiring conductor formed by electroplating can be kept to not more than ±10%.

Presuming that the wiring conductor of copper has a cross-sectional area of a square shape (20 μm×20 μm), and that the thickness produced by the above-mentioned electroless plating is 5 μm, when one set of signal layers, comprising the via hole layer, the X-direction wiring layer, the via hole layer, the Y-direction wiring layer and the via hole layer, is to be formed, the metallic undercoat film, serving as the electrode, must be provided at the lowermost layer over the entire surface of the substrate. However, in this case, the metallic undercoat films at those layers above the lowermost layer need only to be formed at those portions immediately beneath the conductors, and do not need to be formed over the entire area of the substrate. Therefore, except for the metallic undercoat film at the lowermost layer, the metallic undercoat films at those layers above the lowermost layer do not need to be removed after the formation of the thin film multilayer construction.

Instead of using the electroless plating as described above, the thickness of the metallic undercoat film may be increased using a dry process such as vapor deposition, sputtering and ion-plating.

Even with the method of the present invention, when more than several wiring layers are laminated, variations in the thickness of the wiring conductor precipitated by electroplating may sometimes become more than 10%, which is not acceptable. In such a case, it is necessary to provide the metallic undercoat film over the entire area of the substrate so as to obtain the equipotential for the electroplating. In this case, the metallic undercoat film must be etched and removed after the predetermined multilayer process is finished. Therefore, although the metallic undercoat film is provided at the l wer layer, the layer at which the metallic undercoat film is formed is not always limited to the lowermost layer.

In the conventional method, the photoresist is coated, and the grooves are formed, and the wiring conductor is filled in the grooves by electroplating, and thereafter the photoresist is dissolved and removed by a solvent. The steps of the formation and removal of the photoresist are needed so as to etch and remove the metallic undercoat film formed therebelow over the entire area of the substrate. Therefore, it is unnecessary to remove the metallic undercoat film by etching after the formation of the wiring conductor, except at that layer providing the common electrode of the plating, since the photoresist does not need to be used as the plating resist, and the permanent (insoluble) insulating film, which remains from the beginning to the end of the process, can be used. Namely, a disadvantageous treatment for replacing the photoresist by the permanent insulating film can be omitted. And besides, the step of flattening the rugged portion of the permanent insulating film by grinding and polishing in the conventional method is omitted.

The insulating film at the wiring layer (1 t 200 μm) having the metallic undercoat film over the entire area of the substrate is composed of a high thermal-resistant, high glass transition temperature polymer which can be dissolved and removed by a solvent such as an rdinary organic solvent, an alkali aqueous solution, and an organic base (e.g., hydrazine hydrate). The insulating film laminated above this wiring layer should not be dissolved by the above solvent, and should not be adversely affected by this solvent during the dissolving of the soluble insulating film. The soluble insulating film is required to withstand the influence of the curing of the upper insoluble insulating film and its curing temperature, and should not be deteriorated by these factors.

After the soluble insulating film is dissolved and removed by the solvent, an etchant such as cerium (IV) ammonium sulfate dihydrate is caused to intrude into the space formed as a result of removal of this soluble insulating film, thereby removing the metallic undercoat film by etching.

As will be readily appreciated, the reason for the use of the soluble insulating film as described above is to facilitate the etching removal of the metallic undercoat film (over the entire area of the substrate) after the formation of the thin film multilayer construction. Any material other than the soluble insulating film can be used so long as it produces similar effects. One example of such material is a metallic material capable of selective etching, which is different in kind from the wiring conductor. If the wiring conductor is made of copper, zinc capable of selective etching with respect to it is selected. With this method, an electrically-isolated wiring, that is, a floating pattern conductor, can be formed at a desired layer.

The space, formed as a result of removing the soluble insulating film and the metallic undercoat film, produces the effect of increasing the signal transfer speed because of a low dielectric constant; however, an insulating treatment is applied to this space so that contaminants will not intrude into this space. This insulating treatment may be carried out by pouring varnish. The varnish to be used may be either of the solvent type and the non-solvent type.

As described above, the multilayer wiring construction can be produced by sequentially forming a plurality of layers by electroplating, and in this manner a module board required for a computer or the like can be produced.

The various materials used in the thin film multilayer wiring board-producing method of the present invention will now be described.

As the insoluble permanent insulating film, there can be used polyimide, polyamide, polyamide-imide, a cyanate ester resin, an epoxy resin, and an isocyanate-oxazoridone resin which have a high thermal resistance (capable of withstanding the process temperature during the connection and production of the multilayer construction), a high glass transition temperature and a high adhesive property. However, the insoluble insulating film is not limited to these materials.

Polyimide to be used may be either of the photosensitive type or the non-photosensitive type, and may not be limited to a specific chemical structure. However, the polyimide should preferably have a high thermal decomposition temperature (not less than 200° C. and preferably not less than 280° C.), a high glass transition temperature (not less than 200° C. and preferably 280° C.) and a low thermal .expansi n coefficient (not more

than 20 ppm°C^{-1}). Particularly, the type f polyimide, which contains, as an essential component, anhydride having biphenyl moiety or terphenyl moiety, or a diamine having biphenyl moiety or terphenyl moiety, is most preferred.

Polyimide is excellent in all of the above physical properties, but poses some problems. More specifically, the curing temperature must be finally as high as 350° to 400° C. Since it is supplied in the form of a solvent varnish, it is necessary to volatilize the solvent when cured, and therefore pin holes inevitably develop in the insulating film. Polyimide can not be coated into a desired thickness (for example, 20 μm) of the wiring layer at a time, and therefore it must be coated two to three times, and the time required for the curing is more than several hours.

On the other hand, an epoxy resin can be supplied in a non-solvent condition (that is, this resin is not dissolved in a solvent), and a coating without pin holes can be formed. Besides the epoxy resin has a curing temperature of 150° to 200° C. which is much lower than that f polyimide, and therefore the curing time is short. Although there are these advantages, the epoxy resin is inferior in physical properties to the polyimide. More specifically, the conventional epoxy resin has a low thermal decomposition temperature and a low glass transition temperature both of which are less than 200° C. and a high thermal expansion coefficient. Under these circumstances, the inventors of the present invention have made an extensive study, and have found the following facts. A cured substance of an epoxy compound which contains a curing agent having diamino diphenyl methane, diamino diphenyl sulfone, biphenyl moiety or terphenyl moiety, and naphthalene moiety, as well as a cured substance of an epoxy resin having imide moiety, has a thermal decomposition temperature of not less than 300° C. and a glass transition temperature of not less than 300° C., and these substances well satisfy the required thermal resistance of a module board for a computer. The inventors of the present invention also have found the epoxy resin which is lower in thermal expansion coefficient than that of the conventional type, and this epoxy resin, when cooperating with a copper conductor to form a composite structure, is much lowered in thermal stress. Further, this epoxy resin is several times higher in adhesive strength than polyimide. Therefore, depending on the purpose of use of the module, the epoxy resin is suitably used as the insulating film of the thin film multilayer wiring board because of its shortened production time, the structure without pin holes and the high adhesive properties. Particularly when the substrate is thick, much time is required for the temperature rise and the heat radiation for cooling, because such a substrate has a large thermal capacity. In such a case, the non-solvent type epoxy resin which can be cured at low temperatures is very suitable. It is not always necessary to use the permanent insulating film and the soluble insulating film in the form of varnish, and they can be applied to the board of the present invention in the form of a film-like material made of polyimide, polyamide, polyamide-imide, polyester, polycarbonate or the like. In this case, particularly, there is an advantage that there can be selected a suitable permanent insulating film well matching the board f the invention in various properties such as the thermal decomposition temperature, the glass transition temperature and the thermal expansion coefficient. One example of such film material is a polyimide film which contains biphenyl moiety or terphenyl moiety in its molecule, and has a high thermal resistance, a high glass transition temperature and a low thermal expansion coefficient. Usually, the above film-like material can not be bonded to the substrate, and therefore is used in the form of a film with an adhesive of acrylic resin or epoxy resin, or in the form of a B-stage film. Before laminating the layers, grooves for filling the conductor therein may be formed in this film-like insulating material at a place off the production line, and also the metallic undercoat film may be formed. This is very effective in reducing the time of production of the thin film multilayer wiring board.

The soluble insulting film is not limited to the above-mentioned materials, and it may be formed by chemically modifying the above permanent insulating film to impart a solubility thereto. For example, a high molecular-weight phenol novolac and a phenoxy resin may be used.

The grooves, in which the conductor is to be filled by plating so as to form the wiring conductors of the via hole layers (the through hole layers), the X-direction wiring layer, the Y-direction wiring layer and the ground layer, must be formed in the above permanent insulating film. The grooves can be formed by a laser process, a plasm process or a photolithograpy, but can be formed by any other suitable process.

The metallic undercoat film has electrical conductivity so that it can serve as the electrode for the electroplating or as the undercoat for the electroless plating. For example, the metallic undercoat film can be formed using vapor deposition, sputtering, ion plating, electroplating and electroless plating either alone or in combination. In this case, for example, the metallic undercoat film is constituted by a metal layer or multilayer, such as Cr/Cu/Cr, Ti/Cu/Ti, Ti, Cu, Zn, Sn, Co, Fe, Ni, Ni/Cu, Rh, and In.

As the wiring conductor metal, conventional metal with a low resistivity, such as Au, Ag and Cu, can be used.

The present invention will now be described in detail by way of the following Examples.

EXAMPLE 1

FIGS. 4A–4J shows the sequence of steps of a method of producing a thin film multilayer wiring board according to the present invention. In FIGS. 4A–4J, a conductor is filled in grooves by electroplating.

In FIG. 4A, a metallic undercoat film 42 of Cr/Cu having a thickness of 0.8 μm is formed on a ceramics substrate 41 (which may have a multilayer wiring).

In FIG. 4B, a soluble polyimide insulating film 43 having a thickness of 30 μm is coated onto the metallic undercoat film 42 by a spinner, and is finally baked at 350° C. Then, an aluminum film subjected to patterning is formed as a mask on the polyimide film, and grooves 44 are formed in this film by an oxygen plasma, so that the metallic undercoat film 42 is exposed at the bottoms of the grooves 44.

In FIG. 4C, the metallic undercoat film 42 is dipped in an aqueous solution of copper sulfate, and copper is precipitated and filled in the grooves 44 by electroplating, using the metallic undercoat film 42 as an electrode, thereby forming via hole wiring conductors 45.

In FIG. 4D, a metallic undercoat film 42 of Cr/Cu having a thickness of 0.8 μm is formed by sputtering at

those portions disposed immediately beneath an X-layer wiring to be f rmed at an upper layer.

In FIG. 4E, an insoluble polyimide insulating film (permanent insulating film) 46 having a thickness of 20 μm is formed on the upper surface. Then, an aluminum film subjected to patterning is formed as a mask on this polyimide film, and grooves 44 are formed in the polyimide film by an oxygen plasma, so that the metallic undercoat film are exposed at the bottoms of the grooves 44.

In FIG. 4F, since the metallic undercoat film 42 (which is connected to the via hole wiring conductors 45 at the bottoms of the grooves 44), having a pattern corresponding to the pattern of the X-layer wiring, has been exposed, this is dipped in an aqueous solution of copper sulfate, and copper is precipitated and filled in the grooves 44 by electroplating, using the metallic undercoat film as an electrode, thereby forming X-layer wiring conductors 45.

In FIG. 4G, according to the procedure of formation of the X-layer wiring, a via hole layer, a Y-layer, a via hole layer, a ground layer and a via hole layer are sequentially formed in a laminated manner.

In FIG. 4H, the soluble polyimide insulating film 43 is dissolved and removed by a solvent.

In FIG. 4I, the metallic undercoat film 42 at the lowermost layer except for those portions thereof disposed immediately beneath the via hole conductors is etched and removed by cerium (IV) ammonium sulfate dihydrate.

In FIG. 4J, the spaces, formed as a result of removing the soluble polyimide insulating film 43 by dissolving and as a result of removing the metallic undercoat film 42 by etching, are treated with polyimide varnish to insulatively cover the via hole copper.

With the above steps, one set of signal layers have been formed. If necessary, one or more sets of signal layers can be further formed on this first set of signal layers by repeating the steps of FIGS. 4B to 4J.

EXAMPLE 2

In this Example, as in Example 1, a thin film multilayer wiring board is produced according to the method shown in FIGS. 4A–4J. However, in Example 1, the soluble and insoluble insulating films are formed by a liquid material whereas in this Example, film-like materials are used as the insulating films.

In FIG. 4A, a metallic undercoat film 42 of Cr/Cu having a thickness of 0.6 μm is formed by sputtering on a ceramics substrate 41 (which may have a multilayer wiring).

In FIG. 4B, a soluble polyimide film (25 μm thick) 43 with an adhesive is attached to the metallic undercoat film 42, and cured and adhesively bonded thereto. Then, grooves 44, arranged in a pattern corresponding to a via hole pattern, are formed in the polyimide film by ekishima laser through a mask, so that the metallic undercoat film 42 is exposed at the bottoms of the groove 44.

In FIG. 4C, the metallic undercoat film 42 is dipped in an aqueous solution of copper sulfate, and copper is precipitated and filled in the grooves 44 by electroplating, using the metallic undercoat film 42 as an electrode, thereby forming via hole wiring conductors 45.

In FIG. 4D, a metallic undercoat film 42 of Cr/Cu having a thickness f 20 μm is formed by sputtering at those portions disposed immediately beneath an X-layer wiring to be formed at an upper layer, the metallic undercoat film 42 being several μm larger in width than the X-layer wiring.

In FIG. 4E, an insoluble polyimide film (insulating film) (20 μm thick) with an adhesive is bonded to the upper surface, and is cured at 150° C. for several minutes. Then, grooves 44, arranged in a pattern corresponding to an X-layer wiring pattern, are formed in the polyimide film by ekishima laser through a mask, so that the metallic undercoat film 42 is exposed at the bottoms of the holes 44.

In FIG. 4F, since the Cr/Cu metallic undercoat film 42 (which is connected to the via hole wiring conductors 45 at the bottoms of the grooves 44), having a pattern corresponding to the pattern of the X-layer wiring, has been exposed, this is dipped in an aqueous solution of copper sulfate, and copper is precipitated and filled in the grooves 44 by electroplating, using the metallic undercoat film as an electrode, thereby forming X-layer wiring conductors 45.

In FIG. 4G, according to the procedure of formation of the X-layer wiring, a via hole layer, a Y-layer, a via hole layer, a ground layer and a via hole layer are sequentially formed in a laminated manner.

In FIG. 4H, the soluble polyimide insulating film 43 is dissolved and removed by a solvent.

In FIG. 4I, the metallic undercoat film 42 at the lowermost layer except for those portions thereof disposed immediately beneath the via hole conductors is etched and removed by cerium (IV) ammonium sulfate dihydrate.

In FIG. 4J, the spaces, formed as a result of removing the soluble polyimide insulating film 43 by dissolving and as a result of removing the metallic undercoat film 42 by etching, are treated with polyimide varnish to insulatively cover the via hole copper.

With the above steps, one set of signal layers have been formed. If necessary, one or more sets of signal layers can be further formed on this first set of signal layers by repeating the steps of FIGS. 4B to 4J.

EXAMPLE 3

FIGS. 5A–5K shows the sequence of steps of a method of producing a thin film multilayer wiring board according to the present invention. In FIGS. 5A–5K, a conductor is filled in grooves by electroplating or a combination of electroless plating and electroplating.

In FIG. 5A, a metallic undercoat film 52 of Cr/Cu having a thickness of 0.8 μm is formed by sputtering on a ceramics substrate 51 (which may have a multilayer wiring).

In FIG. 5B, a soluble polyimide insulating film 53 having a thickness of 30 μm is coated on the metallic undercoat film 52 by a spinner, and is finally baked at 350° C. Then, an aluminum film subjected to patterning is formed as a mask on the polyimide film, and grooves 54 are formed in the polyimide film by an oxygen plasma, so that the metallic undercoat film 52 is exposed at the bottoms of the grooves 54.

In FIG. 5C, the metallic undercoat film 52 is dipped in an aqueous solution of copper sulfate, and copper is precipitated and filled in the grooves 54 by electroplating, using the metallic undercoat film 52 as an electrode, thereby forming via hole wiring conductors 55.

In FIG. 5D, a metallic undercoat film 52 of Cr/Cu having a thickness of 0.8 μm is formed by sputtering at those portions disposed immediately beneath an X-layer wiring to be formed at an upper layer.

In FIG. 5E, an insoluble polyimide insulating film (permanent insulating film) 56 having a thickness of 20 μm is formed on th upper surface. Then, an aluminum film subjected to patterning is formed as a mask on the polyimide film, and grooves 54 are formed in the polyimide film by an oxygen plasma, so that the metallic undercoat film is exposed at the bottoms of the grooves 54.

In FIG. 5F, copper is filled in the grooves 54 by electroless plating to form electroless-plating conductors 57 having a thickness of 5 μm.

In FIG. 5G, electroplating is further carried out using the metallic undercoat film 52 of Cr/Cu (which is connected to the via hole wiring copper at the bottoms of the groove 54) having a pattern corresponding to an X-layer wiring pattern, thereby forming X-layer wiring conductors 55.

In FIG. 5H, an insoluble polyimide insulating film (permanent insulating film) 56 having a thickness of 20 μm is formed on the upper surface. Then, an aluminum film subjected to patterning is formed as a mask on the polyimide film, and grooves are formed in the polyimide film by an oxygen plasma. Then, the X-layer wiring conductors exposed in the grooves are dipped in an aqueous solution of copper sulfate, and copper is precipitated and filled in the grooves by electroplating, using these wiring conductors, thereby forming a via hole layer. An insoluble polyimide insulating film (permanent insulating film) 56 having a thickness of 20 μm is formed on the supper surface. Then, an aluminum film subjected to patterning is formed as a mask on the polyimide film, and grooves are formed in the polyimide film by an oxygen plasm, so that a metallic undercoat film, having a pattern corresponding to a Y-layer wiring pattern, is exposed at the bottoms of the grooves. Copper is precipitated and filled in the grooves by electroless plating to form electroless-plating conductors 57 having a thickness of 5 μm. Further, electroplating is carried out using, as an electrode, the metallic undercoat film 52 of Cr/Cu (which is connected to the via hole conductor copper at the bottoms of the grooves 54) having a pattern corresponding to the Y-layer wiring pattern, thereby forming Y-layer wiring conductors 55. Then, according to the procedure of formation of the X-layer wiring, a via hole layer, a ground layer and a via hole layer are sequentially formed in a laminated manner.

In FIG. 5I, the soluble polyimide insulating film 53 is dissolved and removed by a solvent.

In FIG. 5J, the metallic undercoat film 52 at the lowermost layer except for those portions thereof disposed immediately beneath the via hole conductors is etched and removed by cerium (IV) ammonium sulfate dihydrate.

In FIG. 5K, the spaces, formed as a result of the removal of the soluble polyimide insulting film 53 by dissolving and as a result of removing the metallic undercoat film 52 by etching, are treated with polyimide varnish to insulatively cover the via hole copper.

With the above steps, one set of signal layers have been formed. If necessary, one or more sets of signal layers can be further formed on this first set of signal layers by repeating the steps of FIGS. 5B to 5K.

The metallic undercoat films of the wiring pattern for the electroless plating are provided at the X-layer and Y-layer, respectively, and these undercoat films need to be provided at least at those portions disposed immediately beneath the wiring conductors, but do not need to be provided over the entire surface. The via hole conductors are disposed in the ground layer in electrically interrupted relation to the ground layer, and are electrically connected to the Y-layer wiring beneath this ground layer. Therefore, the metallic undercoat film (serving as the common electrode) at the lowermost layer is not electrically connected to the metallic undercoat film at the ground layer, and therefore it is necessary to electrically connect the two together from the exterior.

EXAMPLE 4

FIGS. 6A–6K shows the sequence of steps of a method of producing a thin film multilayer wiring board according to the present invention. In the method of FIGS. 6A–6K, the step of forming a material capable of selective etching is added to the method of FIGS. 4A–4J.

In FIG. 6A, a metallic undercoat film 62 of Ni/Cu having a thickness of 0.8 μm is formed by sputtering on a ceramics substrate 61 (which may have a multilayer wiring).

In FIG. 6B, a photoresist 63 having a thickness of 22 μm is coated on the metallic undercoat film 62 by a spinner, and grooves 64 are formed by exposure and development, so that the metallic undercoat film 62 is exposed at the bottoms of the grooves 64.

In FIG. 6C, the metallic undercoat film 62 is dipped in an aqueous solution of copper sulfate, and copper is precipitated and filled in the grooves 64 by electroplating, using the metallic undercoat film 62 as an electrode, thereby forming via hole wiring conductors 65.

In FIG. 6D, the photoresist 63 is entirely dissolved and removed by a solvent.

In FIG. 6E, Zn 67 is precipitated and filled in those portions, from which the photoresist 63 has been removed, by electroplating using the metallic undercoat film 62 as an electrode, thereby forming via hole wiring conductors 65. The Zn 67 precipitated on the via hole wiring 65 is removed, and the rinsing is carried out. With this procedure, the warp of the ceramics substrate 61 was greatly reduced.

In FIG. 6F, an insoluble polyimide insulating film (permanent insulating film) 66 having a thickness of 22 μm is coated on the upper surface by a spinner, and is heated and cured. Then, grooves for forming an X-layer wiring are formed by ekishima laser, and the Zn 67 and the via hole wiring conductors 65 are exposed.

In FIG. 6G, since the Zn 67 and the via hole wiring conductors 65 have been exposed at the bottoms of the grooves 64, they are dipped in an aqueous solution of copper sulfate, and copper is precipitated and filled in the grooves 64 by electroplating using them as an electrode, thereby forming X-layer wiring conductors 65.

In FIG. 6H, an insoluble polyimide insulating film (permanent insulating film) 66 having a thickness of 20 μm is formed on the upper surface. Grooves are formed in the polyimide film by ekishima laser, and the X-layer wiring conductors 65 exposed in the grooves are dipped in an aqueous solution of copper sulfate, and copper is precipitated and filled in the grooves by electroplating using the exposed conductors 65 as an electrode, thereby forming a via hole layer. An insoluble polyimide insulating film (permanent insulating film) 66 having a thickness of 20 μm is formed on the upper surface. Grooves are formed by ekishima laser, so that a metallic undercoat film is exposed at the bottoms of the grooves. Electroplating is carried out using, as an elec-

trode, the metallic undercoat film 62 of Cr/Cu (which is connected to the via hole conductor copper at the bottoms of the grooves 64) having a pattern corresponding to a Y-layer wiring pattern, thereby forming Y-layer wiring conductors 65. Then, according t the procedure of formation of the X-layer wiring, a via hole layer, a ground layer, a via hole layer are sequentially formed in a laminated manner.

In FIG. 6I, Zn 67 is etched and removed, and the rinsing is carried out.

In FIG. 6J, the metallic undercoat film 62 at the lowermost layer except for those portions thereof disposed immediately beneath the via hole conductors is etched and removed by cerium (IV) ammonium sulfate dihydrate.

In FIG. 6K, the spaces, formed as a result of removing the Zn 67 and the metallic undercoat film 62 by etching, are treated with polyimide varnish to insulatively cover the Via hole copper.

With the above steps, one set of signal layers have been formed. If necessary, one or more sets of signal layers can be further formed on this first set of signal layers by repeating the steps of FIGS. 6B to 6K.

The metallic undercoat films of the wiring pattern for the electroplating are provided at the X-layer and Y-layer, respectively, and these undercoat films need to be provided at least at those portions disposed immediately beneath the wiring conductors, but do not need to be provided over the entire surface. The via hole conductors are disposed in the ground layer in electrically interrupted relation to the ground layer, and are electrically connected to the Y-layer wiring beneath this ground layer. Therefore, the metallic undercoat film (serving as the common electrode) at the lowermost layer is not electrically connected to the metallic undercoat film at the ground layer, and therefore it is necessary to electrically connect the two together from the exterior when carrying out the electroplating.

EXAMPLE 5

In this Example, as in Example 4, a thin film multilayer wiring board is produced according to the method of FIGS. 6A–6K. However, in this Example, Zn 67 is not precipitated on the via hole wiring conductors 65 of Example 4.

In FIG. 6A, a metallic undercoat film 62 of Ni/Cu having a thickness of 0.8 μm is formed by sputtering on a ceramics substrate 61 (which may have a multilayer wiring).

In FIG. 6B, a photoresist 63 having a thickness of 22 μm is coated on the metallic undercoat film 62 by a spinner, and grooves 64 are formed by exposure and development, so that the metallic undercoat film 62 is exposed at the bottoms of the grooves 64.

In FIG. 6C, the metallic undercoat film 62 is dipped in an aqueous solution of copper sulfate, and copper is precipitated and filled in the grooves 64 by electroplating, using the metallic undercoat film 62 as an electrode, thereby forming via hole wiring conductors 65.

In FIG. 6D, a thin film of a surface active agent containing fluorine is coated on the entire surfaces of the via hole wiring conductors 65, and is baked thereto. The photoresist 63 except for those portions thereof around the via hole wiring conductors 65 is dissolved and removed by a solvent.

In FIG. 6E, the metallic undercoat film 62 is dipped in an aqueous solution of copper sulfate, and Zn 67 is precipitated and filled in those portions, from which the photoresist 63 has been removed, by electroplating using the metallic undercoat film 62 as an electrode, thereby forming via hole wiring conductors 65. With this procedure, the warp of the ceramics substrate 61 was greatly reduced.

In FIG. 6F, an insoluble polyimide insulating film (permanent insulating film) 66 having a thickness of 22 μm is coated on the upper surface by a spinner, and is heated and cured. Then, grooves for forming an X-layer wiring are formed by ekishima laser, and the Zn 67 and the via hole wiring conductors 65 are exposed.

In FIG. 6G, since the Zn 67 and the via hole wiring conductors 65 have been exposed at the bottoms of the grooves 64, they are dipped in an aqueous solution of copper sulfate, and copper is precipitated and filled in the grooves 64 by electroplating using them as an electrode, thereby forming X-layer wiring conductors 65.

In FIG. 6H, an insoluble polyimide insulating film (permanent insulating film) 66 having a thickness of 20 μm is formed on the upper surface. Grooves are formed in the polyimide film by ekishima laser, and the X-layer wiring conductors 65 exposed in the grooves are dipped in an aqueous solution of copper sulfate, and copper is precipitated and filled in the grooves by electroplating using the exposed conductors 65 as an electrode, thereby forming a via hole layer. Further, an insoluble polyimide insulating film (permanent insulating film) 66 having a thickness of 20 μm is formed on the upper surface. Grooves are formed by ekishima laser, so that a metallic undercoat film is exposed at the bottoms of the grooves. Electroplating is carried out using, as an electrode, the metallic undercoat film 62 of Cr/Cu (which is connected to the via hole conductor copper at the bottom of the grooves 64) having a pattern corresponding to a Y-layer wiring pattern, thereby forming Y-layer wiring conductors 65. Then, according to the procedure of formation of the X-layer wiring, a via hole layer, a ground layer, a via hole layer are sequentially formed in a laminated manner.

In FIG. 6I, Zn 67 is etched and removed, and the rinsing is carried out.

In FIG. 6J, the metallic undercoat film 62 at the lowermost layer except for those portions thereof disposed immediately beneath the via hole conductors is etched and removed by cerium (IV) ammonium sulfate dihydrate.

In FIG. 6K, the spaces, formed as a result of removing the Zn 67 and the metallic undercoat film 62 by etching, are treated with polyimide varnish to insulatively cover the via hole copper.

With the above steps, one set of signal layers have been formed. If necessary, one or more sets of signal layers can be further formed on this first set of signal layers by repeating the steps of FIGS. 6B to 6K.

The metallic undercoat films of the wiring pattern for the electroplating are provided at the X-layer and Y-layer, respectively, and these undercoat films need to be provided at least at those portions disposed immediately beneath the wiring conductors, but do not need to be provided over the entire surface. The via hole conductors are disposed in the ground layer in electrically interrupted relation to the ground layer, and are electrically connected to the Y-layer wiring beneath this ground layer. Therefore, the metallic undercoat film (serving as the common electrode) at the lowermost layer is not electrically connected to the metallic undercoat film at the ground layer, and therefore it is neces-

sary to electrically connect the two together from the exterior when carrying ut the electroplating.

EXAMPLE 6

FIGS. 7A–7J shows the sequence of a method of steps of producing a thin film multilayer wiring board according to the present invention. In the method of FIGS. 7A–7J, unlike Examples 1 to 5, a step of the method is applied to a lower surface of a substrate. A metallic film is formed over an entire surface of a ceramics substrate to made all of I/O pin-side terminals conductive.

In FIG. 7A, a film of Cr (0.05 μm) and a film of Cu (0.5 μm) are formed by sputtering on an entire lower surface (I/O pin-side surface) of an alumina substrate 71 (which may have a multilayer wiring) of a square shape (100 mm×100 m; thickness: 1 mm) to thereby provide a metallic film 73 of Cr/Cu. This Cr/Cu metallic film is used as a common electrode at a later stage. The wiring of the alumina substrate 71 is constituted only by through hole wiring conductors.

In FIG. 7B, a metallic undercoat film 74 of Cr/Cu having a thickness of 0.8 μm is formed by sputtering on those portions of the upper surface of the alumina substrate 71 (100 mm×100 mm; thickness: 1 mm) on which ground conductors and via hole conductors are to be formed.

In FIG. 7C, an insoluble polyimide film 75 (20 μm thick) with an epoxy adhesive is bonded to the upper surface, and is cured. Then, grooves, arranged in a pattern corresponding to the patterns of the ground and the via holes, are formed in the polyimide film by ekishima laser through a mask, so that the metallic undercoat film 74 is exposed at the bottom of the grooves.

In FIG. 7D, the metallic undercoat film 74 is dipped in an aqueous solution of copper sulfate, and copper is precipitated and filled in the grooves by electroplating using the metallic undercoat film 74 as an electrode, thereby forming via hole wiring conductors 76 and ground wiring conductors 77.

In FIG. 7E, an insoluble polyimide film with an epoxy adhesive is bonded, and heated and cured, and grooves, arranged in a pattern corresponding to a via hole pattern, are formed in the polyimide film by ekishima laser through a mask. Using an aqueous solution of copper sulfate, electroplating is carried out using the via hole conductors (disposed below this polyimide film) as an electrode, thereby forming via hole conductors to form a via hole conductor layer 79.

In FIG. 7F, a metallic undercoat film 74 of Cr/Cu, having a pattern corresponding to an X-layer wiring pattern, is formed by sputtering.

In FIG. 7G, an insoluble polyimide film with an epoxy adhesive is bonded, and heated and cured. Grooves, arranged in a pattern corresponding to the X-layer wiring pattern, are formed in the polyimide film by ekishima laser. Using an aqueous solution of copper sulfate, X-layer wiring conductors are precipitated by electroplating using the metallic undercoat film 74 as an electrode, thereby forming X-layer wiring conductors 701.

In FIG. 7H, via hole conductors 79 are formed according to the above procedure.

In FIG. 7I, according to the above procedure, a Y-layer wiring layer 702, a via hole conductor layer 79, an upper ground layer 78 and a via hole conductor layer 79 are sequentially formed.

In FIG. 7J, the Cr/Cu metallic film 73 on the lower surface f the substrate is etched and rem ved by cerium (IV) ammonium sulfate dihydrate, thereby completing one set of signal layers.

EXAMPLE 7

Modules are produced using the thin film multilayer wiring boards produced in Example 2 and Example 6. FIG. 8 shows the module using the thick and thin film multilayer wiring board (having thick layers and thin layers) of Example 2. FIG. 9 shows the module using thin film multilayer wiring board (all layers are thin) of Example 6.

High-temperature solder 83 is placed on each of pin-connecting pads 82 formed on the reverse surface of the thick and thin film multilayer wiring board 81 produced in Example 2. A pin 84, which is heated to about 350° C. only at its connecting portion and is received in a guide hole, is connected and secured to the pad 82 through the solder 83. Then, solder 85 is placed on each of semiconductor-mounting pads formed on the front surface of the board, and is heated to a temperature of about 250° C., and four LSIs 86 are electrically connected and secured to these pads through the solder 85. Then, a rubber plate 87, having electrical conductivity, a good thermal conductivity and heat resistance, is adhesively bonded to the reverse surface of each LSI. Finally, low-temperature solder is placed on a solder seal portion on the surface of the board, and is heated to about 200° C., and a covar seal cap, having an integral cooling fan 88 for cooling the LSIs, is connected to the solder seal portion through the solder in such a manner that the inner surface of the seal cap is held in contact with the rubber plate 87, thereby completing the module.

Similarly, the module is produced using the thin film multilayer wiring board of Example 6.

One of the above four LSIs is a logic LSI, and the other three are memory LSIs.

EXAMPLE 8

A computer is produced using the modules of Example 7. FIG. 10 shows a logic package of the computer using the modules of Example 7.

In FIG. 10, sixteen (16) modules 101 of Example 7 are mounted on a printed circuit board 102 to form the logic package of the computer. Then, a memory package and an input/output processing package are combined with this logic package to form the computer.

COMPARATIVE EXAMPLE 1

The conventional method of producing the thin film multilayer wiring board has the problem that the time for producing the wiring board is long, and also has the problem that the substrate is warped. Namely, while the polyimide films are repeatedly formed, the substrate is warped due to stresses developing in the interior. This warp adversely affects the grinding and polishing operation for flattening purposes. Also, the warp makes it difficult to perform the exposure of a large-area substrate at a time, and therefore the exposure must be done by a step-and-repeat method, which is a major factor in lowering a throughput. In a board for a high-speed transfer circuit of a computer, it is preferable that the substrate be provided with the smallest thickness. Preferably, this thickness should be not more than 1 mm, and under the circumstances, it is difficult to prevent the warp of the substrate by increasing the thickness of the substrate.

FIG. 11 shows the relation between the thickness of a polyimide film (PIQ; manufactured by Hitachi Kasei K. K.) and a warp of a substrate. Polyimide varnish PIQ is coated in up to 32 layers (each having a thickness of 12.5 mm after baking) on an alumina substrate (thickness: 1 mm; square shape (100 mm×100 mm); elastic modulus: 35×10^{10}Pa; Poisson's ratio v: 0.27). The standard baking conditions are adopted. Namely, the baking time is 30 minutes, and the baking temperature is 140° C., 200° C. and 350° C. The warp of the substrate on the thin film side was measured using a wide-range thin film step meter. The warp of the substrate reaches a large value of 180 μm when the thickness of the polyimide film is 400 μm. Namely, in the exposure and development step, when the warp is large, a fuzz or haze develops in the transfer of a mask pattern, so that a proper pattern transfer can not be effected, which prevents a high-precision design of the circuit. It has been confirmed by our experiments that the allowable upper limit for the warp is 10 μm. Therefore, unless the warp of the substrate is greatly reduced, the number of layers to be formed can not be increased in the conventional method. This is a major obstacle to the demand for the multilayer construction.

On the other hand, in the present invention, when a plurality of layers are to be formed on the same substrate as described above, using polyimide films (film-like material) (20 μm thick) each having an epoxy resin adhesive (1 to 3 μm thick), thermal stresses are so small as to hardly cause a warp, because even if the films have the same nature as PIQ, the thickness of the adhesive layer is very thin, and the epoxy resin can be cured at low temperatures of not more than 100° C. If the film is compressed and bonded by a hot press of an excellent flatness, the flatness of the surface of the hot press is transferred to the film, and the substrate is not warped. Therefore, with the film bonding method of the present invention, the multilayer construction can be suitably achieved, and in the present invention, the multilayer construction having up to 100 layers can be achieved, whereas in the conventional method, the upper limit of the multilayer construction is 10 layers or so.

Further, the polyimide is used in the cured form (that is, in the form of a film material), and therefore unlike the varnish polyimide, the polyimide film, having a thermal expansion coefficient (3 to 10 ppm°C^{-1}) several times lower than that of PIQ, can be used. As the thermal expansion coefficient of polyimide decreases, a problem arises in that the polyimide film can not be bonded to the substrate and another polyimide film. The limit of the thermal expansion coefficient in this case is about 10° to 18° $C.^{-1}$. When the polyimide is used in the form of a film material as described above, the adhesive bonding is carried out not by mutual fusion of the polyimide molecules, but by the epoxy resin having an extremely higher adhesive strength than the polyimide. The range of choice of the epoxy resin is wide, and a considerable degree of freedom is obtained with respect to its choice, and the thickness of the adhesive layer is extremely small, and even if the thermal expansion coefficient of the polyimide is greatly decreased, this will not adversely affect the adhesive bonding because the adhesive bonding is carried out by the epoxy resin. Incidentally, instead of using the polyimide film having the epoxy resin coated thereon, an epoxy resin may be coated on the substrate in which case the polyimide film is bonded to this epoxy resin.

As described above, the film bonding method of the present invention is quite effective in decreasing the thermal stresses, and can contribute to the reduction of the warp and the multilayer construction.

What is claimed is:

1. A thin film multilayer wiring board-producing method comprising the steps of:

(1) forming a first metallic undercoat film on a substrate, then forming a soluble insulating film on said metallic undercoat film, forming grooves in said soluble insulating film so that at least a part of the metallic undercoat film is exposed at the bottom of each of the grooves, and then filling a first conductor in said grooves by electroplating, thereby forming a first layer;

(2) subsequently forming an insoluble insulating film on said first layer or on a patterned metallic undercoat film formed on said first layer, which metallic undercoat film is electrically connected to said conductor provided in the first layer, forming grooves in said insoluble insulating film so that at least a part of the first layer or the metallic undercoat layer formed on said first layer is exposed at the bottom of each of the grooves, and then filling a second conductor in said grooves by the use of electroplating or both electroless plating and electroplating, thereby forming a second layer on said first layer or on the metallic undercoat film formed on said first layer; and

(3) subsequently removing said soluble insulating film and a part of said first metallic undercoat film which is exposed, and then forming an insoluble insulating film at those portions from which said soluble insulating film and said first metallic undercoat film have been removed.

2. A thin film multilayer wiring board-producing method comprising the steps of:

(1) forming a first metallic undercoat film on a substrate, then forming a soluble insulating film on said metallic undercoat film, forming grooves in said soluble insulating film so that at least a part of the metallic undercoat film is exposed at the bottom of each of the grooves, and then filling a first conductor in said grooves by electroplating, thereby forming a first layer;

(2) subsequently forming an insoluble insulating film on said first layer or on a patterned metallic undercoat film formed on said first layer, which metallic undercoat film is electrically connected to said conductor provided in the first layer, forming grooves in said insoluble insulating film so that at least a part of the first layer or the metallic undercoat layer formed on the first layer is exposed at the bottom of each of the grooves, and then filling a second conductor in said grooves by the use of electroplating or both electroless plating and electroplating, thereby forming a second layer on said first layer or on the metallic undercoat layer formed on the first layer;

(3) subsequently repeating said step (2) one or more times to provide a multilayer construction; and

(4) subsequently removing said soluble insulating film and a part of said first metallic undercoat film which is exposed, and forming an insoluble insulating film at those portions from which said soluble insulating film and said first metallic undercoat film have been removed.

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